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Design and Implementation of Programmable Hearing Aid Using FPAA

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Abstract. This work proposes cost effective custom design programmable hearing aid and implement it using FPAA (Field programmable analog array). FPAA has programmable analog module used to implement the reconfigurable filters and amplifier to correct impaired hearing loss according to the individual's audiogram. Presently, the available analog and digital hearing aid has uniform gain over entire range audiogram, which is not a desirable requirement. In this work programmable analog processor is configured based on the individual's audiometry. The audiometry is divided into small sub bands based on the hearing loss profile. Filters and amplifiers are configured with the suitable gain to compensate the hearing loss at different sub bands. The parameters of the desired circuit are optimized through simulation using P-spice and Anadigm designer2 tools. Optimized parameters are loaded in the AN231E04 FPAA hardware module. Prototype custom design designed processor has four sub bands, which are tested with the standard test input signal and also implemented for the real data obtained from three case studies and hearing loss compensation is successfully implemented.

Keywords: programmable filter, customized analog processor, FPAA, programmable hearing aid, ASIC.

1 INTRODUCTION

Hearing is one among the five sense of human being. It is estimated that 42% of the people suffering with hearing loss and impairment. This work proposes to design a custom programmable cost effective hearing aid to suit individual's requirement. A conventional hearing instrument essentially consists of a microphone, battery, an amplifier and a loud speaker. The main task of hearing aid devices is to amplify sounds signal and transfer it to the ear [1].The acoustical signal captured by the microphone is amplified and is fed to the ear phone. Recently, digital hearing aids are designed and developed have more advantage than analog hearing aids because it has low power consumption, small size and low noise. Digital hearing instruments [1], [2] uses advanced digital signal processing like multichannel compression, multiple memories and intelligent signal processing, which improves the

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performances of the hearing instruments and the satisfaction of the user. With the development of VLSI microelectronics technology, it is now possible to incorporate greater function modules of electronic circuits in a very small area, and hearing instruments now can be positioned completely inside the ear canal [3].

An audiogram is a graph that shows the softest sounds a person can hear and the sounds are measured at different frequencies (pitches). Usually, the hearing levels (HLs) are measured at octave frequencies like 125/250/500/1k/2k/4k/8k Hz, and used in the fitting process of hearing aids [2], [4]. If a person's threshold hearing loss (HL) is within or below the 'banana' shape, some sounds cannot be heard. This hearing loss must be compensated through using hearing aid for smooth conversation. The patterns of audiograms differ from person to person, and one typical hearing loss pattern is due to aging. For patients with hearing loss less than 90 dB, a conventional hearing aid could be efficient in restoring the hearing [5].

In the present technology, cost of the digital hearing aid is very high. ASIC designing cost is high due to complex DSP and filters. FPAA is a reconfigurable analog module used to implement the reconfigurable filters and amplifier to correct impaired hearing loss according to the individual audiometry. This focuses on design of custom designed processor using FPAA, the design and implementation of signal conditioning circuit. Hearing aid should be able to adjust sound levels within a given spectrum. In practice, this is done by passing the input signals to different filter bands that is divided into different pass band frequencies. The gains for each sub bands are adjustable to suit the needs of hearing impaired, i.e. the amplitude response of filter bank should equalize or 'match' the audiogram [4]. So, the patients can take advantage of their specific case to improve their auditive performances.

Due to the high nonrecurring engineering costs of integrated circuit design, rapid-prototyping is an important field in microelectronics. FPAA provides an alternative solution for implementing the digital approximation of analog filters [6]. For digital circuits; FPGAs are highly developed and have become indispensable as both development tool and application platform. In contrast, the nature of analog circuits is much more complex and does not readily allow a mapping of any arbitrary analog behavior to a generic set of basic building-blocks and routing nodes [7]. Therefore, FPAA are very specific to the target application and suffer from performance degradations when compared to single-purpose ASICs. FPAA are the counterparts of the field programmable gate arrays (FPGAs) in analog domain [7]. FPAA is also used in implementing shunt active filter and analog signal processing circuits [8], [9]. Moreover recently arrived FPAA is making the migration of the designs towards Field Programmable Mixed Arrays (FPMA) which are the combination of both FPGA and FPAA.

This paper is organized as follows. In section II, methodology adopted and the sub band filter design for programmable hearing aid are discussed. Section III discuss the implementation of designed circuit in Orcad P-spice, Anadigm environment and real input signal. Section IV discusses the inference from the obtained results with real inputs, followed by the conclusion.

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2 METHODOLOGY

2.1 Study of Audiogram

Audiogram is the study of hearing losses, which can be plotted based on the hearing capability of a person. It is a plot or graph in terms of frequency versus decibels in the range of 125 Hz to 8 kHz. Figure.1 shows the audiogram and the classification of hearing impairment.
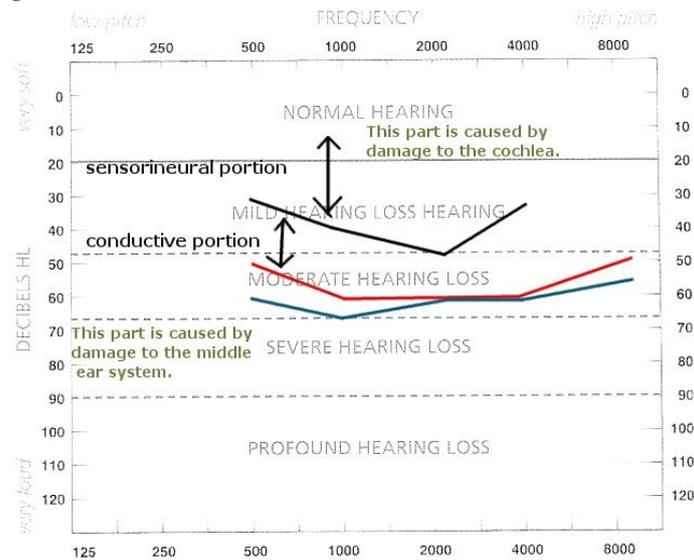
Figure 1. Classification of hearing impairment

The real audiogram data reveals that the patient does not have uniform loss over the selected range. Most of the data shows a hearing loss in particular frequency range with the selected bandwidth. The normal hearing is considered with hearing sensitivity below 20 dB. The hearing loss (HL) beyond 90 dB is considered as permanent loss. The sensitivity between 20 dB to 90 dB is considered as HL.

2.2 Proposed Model of Customized Design Processor

Customized processor is an ASIC processor developed in FPAA for hearing aid application. It consists of filter and amplifier bank and mixer, finally the processed signal is fed to the earphone as shown in Figure 2. Most of the conventional hearing aid amplifies uniformly, which is not the desired response. In order to correct these losses in the selected HL region, programmable hearing aid was developed using FPAA. The proposed hearing aid is a customized analog processor proposed to correct the HL in better and cost effective in comparison with the existing system. Programmable hearing aid using FPAA is designed using multiple filters of different sub-bands of frequency in which amplification and sensitivity can be

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easily controlled by programming the gain for various band of frequency for different hearing loss patterns.
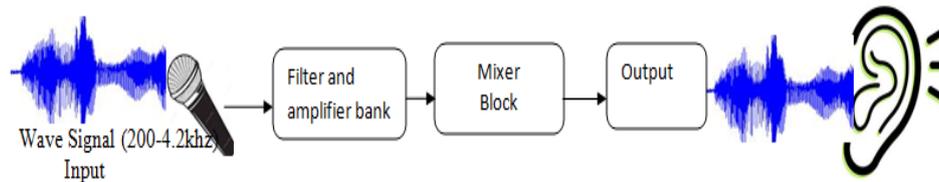

Figure 2. Block diagram of hearing aid application.

The input signal picked from the microphone fed to the programmable filter to reduce the unwanted noise. The filter is divided into four different bandwidth of frequency of audible range between 350 Hz - 4.2 kHz.

2.3   Design of Analog Filter Block

The block diagram of analog processor consists of filter bank and mixer circuit is as shown in Figure 3. Analog signal is input audio signal input to with the filter for the range of frequency from 350 Hz to 4.2 kHz.
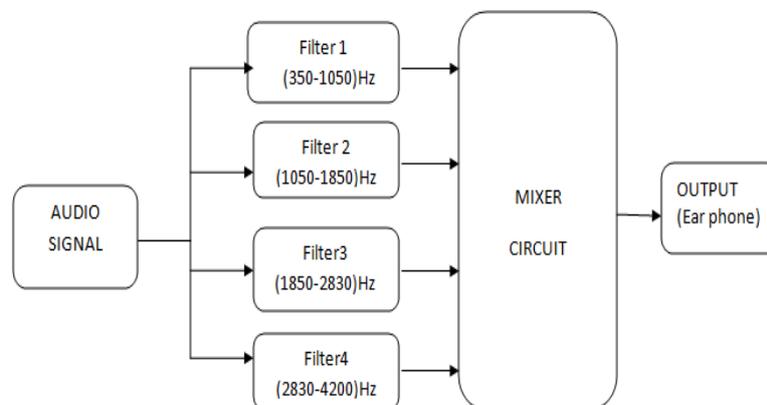

Figure 3. Block diagram of analog filter bank.

Filter Design. A filter is an electric circuit that passes electric signals of certain frequencies ranges, while preventing the passage of others. Filter circuits are used in a wide variety of applications. Active components are used to design BPF, depending on four different bandwidth of frequency. The bandwidth of the filter is simply the difference between the upper and lower cut off frequencies. Active filters are designed using the design equation given by Ron Mancini [10].
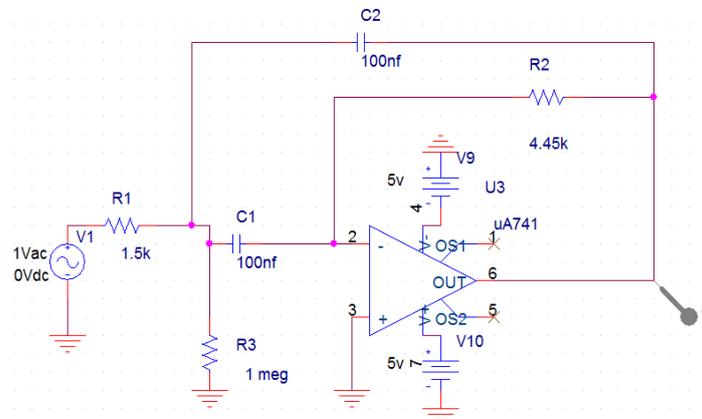
Figure 4. Filter implemented in P-spice.

Filters are designed and implemented in Orcad P-spice to optimize the parameter real time application and using multi feedback (MFB) band pass filter as shown in Figure 4. Filters are divided into four different frequencies of bandwidth are given as, Filter 1: (350-1050) Hz, Filter 2: (1050-1850) Hz, Filter 3: (1850-2830) Hz, Filter 4: (2830-4320) Hz. MFB is used for lower bandwidth of frequencies. The MFB band-pass allows to adjust quality factor (Q), mid frequency gain (Am), and mid frequency of filter (fm) independently. Bandwidth and gain factor do not depend on R3. Therefore, R3 can be used to modify the mid frequency without affecting bandwidth, B, or gain, Am. For low values of Q, the filter can work without R3 however; Q then depends on Am [11].

$$-A_m = 2Q^2 \qquad (1)$$

The other parameters of the filters can be calculated using the formulas given which is as follows:
Mid frequency (fm) of the filter is determined using the formula given below:

$$f_m = \frac{1}{2\pi C} \sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}} \qquad (2)$$

Where, C is capacitance in pF
R is the resistance in ohms

$$-A_m = \frac{R_2}{2R_1} \qquad (3)$$

To calculate the resistance and capacitance value for the filter design, the gain should be greater or equal to 4. Value of the capacitance is constant for all the four filter design which is given by 100 pF, and the resistance values are calculated using the equation (4).

$$R_2 = \frac{Q}{\pi f m C}$$

(4)

$$R_1 = \frac{R_2}{-2A_m}$$

(5)

$$R_3 = \frac{A_m R_1}{2Q^2 + A_m}$$

(6)

Using equation (5) and equation (6) the design values for R1, R3 for different bandwidth of filter ranges from 200 Hz to 4.2 kHz are calculated.

Mixer design. A mixer is a nonlinear electrical circuit that creates new frequencies from two signals applied to it. Active mixers used as amplifying device and isolation between the ports, but may have higher noise and more power consumption. Active mixer is used in this design which is used as amplifying device provides improved isolation, higher noise and power consumption. Figure 5 shows the mixer circuit implementation in P-spice using simple RC network using op-amp μA741.
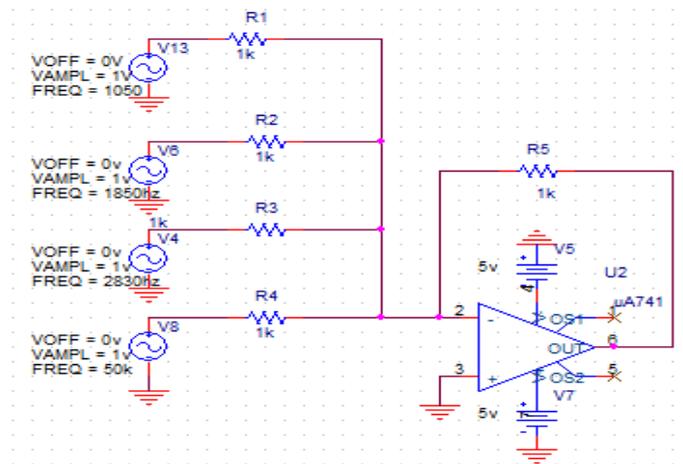

Figure 5. Mixer circuit implementation in Orcad P-spice.

3   IMPLEMENTATION

3.1   Implementation of customized analog processor model in spice

Customized analog processor designed for hearing aid application for the proposed design frequency range is shown in figure 6. The circuit design consists of four

filter banks, whose output signals are amplified using feedback and gain function combined by mixer circuit.
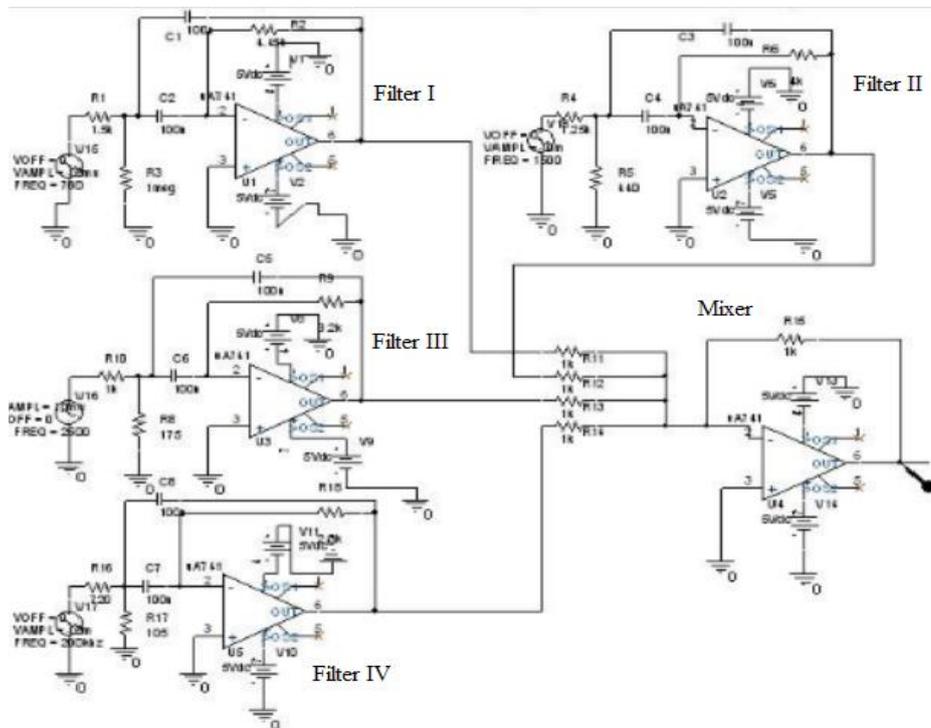

Figure 6. Schematic of customized processor in P-spice.

3.2   Implementation of customized analog processor in Anadigm designer2 software

AN231E04 FPAA processor is used in the implementation of proposed custom designed analog processor. FPAA has switched capacitor circuit operating with operational amplifiers and numerous switches incorporate many classes of interconnections. Important components of the array are programmable capacitor banks, where interconnections and switches are to make proper parallel connections. The CAB (configurable analog blocks) capacitor characteristics do not depend upon the absolute value of the capacitors rather depend on the ratio between them. FPAA can be used to implement various analog functions using CAB and programmable interconnections network. Each CAB can implement a number of analog signal processing functions such as amplification, differentiations, integration, addition, subtraction, multiplication, log, exponential and even analog to digital conversion. The interconnections network routes signal from one CAB to other, and to and from I/O blocks.

Figure 7. Shows the ASIC implemented in Anadigm designer2 software. In FPAA reconfigurable filter is implemented using switched capacitor, in which each

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AN231E04 has four CABS distributed in 2 x 2 arrays. Anadigm designer2 software is used to compile the designed ASIC processor, which is loaded in FPAA for implementation. ASIC circuit builtin FPAA is used to realize a filter bank for the hearing aid. It has biquadratic filter, using CAM parameters are adjusted using Anadigm designer2 simulation tool for reconfiguration. In this implementation two AN231E04 proto board are used due to the limited CAMs in each proto board. Two sum filter and biquad filter are implemented in first proto board and a second proto board is used to implement other two sum filter, two biquad filters and gain inverter. Speech or sound signal acts as input to the sum filter. 1V is given as input for testing and common mode offset voltage of 1.5V is taken to suit the design applications. The input are taken from the signal generators and fed to the sum filters. Three input signal is given to the first sum filter, which has frequency of 250 Hz and unity gain is set for all the three inputs filter i.e. upper, middle and lower. One single input and mixed output is given to the second sum filter with same set specification. The mixed output signal is given as an input to the two different filters present in the first proto board.

Filters has its signal frequency of 250 Hz, gain is equal to one and quality factor of 10 is set as an input parameter for all the four filters except the corner frequency has 0.616 kHz, 1.38 kHz, 2.29 kHz and 4.2 kHz for filter 1 to filter 4 respectively. In second proto board, the outputs from all the filters are fed to the sum filter to combine the filter output and reduce unwanted noise present in the audio signal. In hardware implementation, input is a speech signal fed as input signal and output is listened through audio jack and the unwanted noise signal above 4.2 kHz is suppressed.
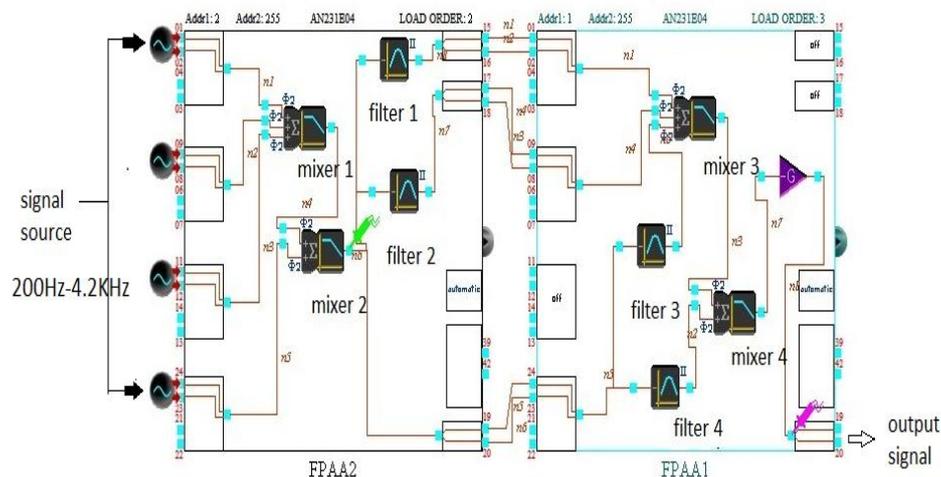

Figure 7. ASIC implementation in Anadigm Designer2 software environment.

Experimental setup for testing the ASIC process implementation in FPAA with real audio signal is shown in the Figure 8. The input signal is a speech signal recorded in .wav format and fed as input. Two FPAA kit are used in this implementation the output signal is fed to the headphone.
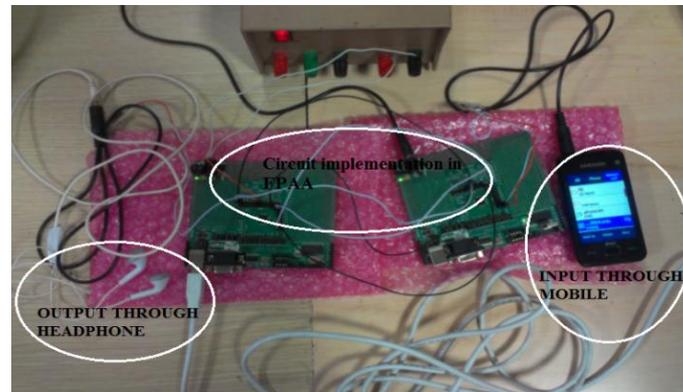
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Figure 8. Experimental set up for testing the ASIC processor in FPAA using audio signal.

3.3 Design for HL correction

Audiogram of patients has been taken for experimentation to correct the hearing loss of patients using programmable hearing aid. Losses can be corrected by varying the gain factor of the particular bands of filter at which losses occur. The gain factor can be calculated using the equation (7) and equation (8). According to the individual patient's requirement, the FPAA is reconfigured.

$$dB = 20 \log (\text{voltage gain}) \qquad (7)$$
$$\text{Voltage gain} = \text{antilog} (dB/20) \qquad (8)$$

4 RESULTS AND DISCUSSION

The audiograms of 3 different patients are taken for case study to correct the HL. Figure 9. shows the experimental set-up for testing the customized process using standard input signal. The standard input signals are taken from function generator and the output is given to CRO which has been carried out to analyze the designed filter characteristics.
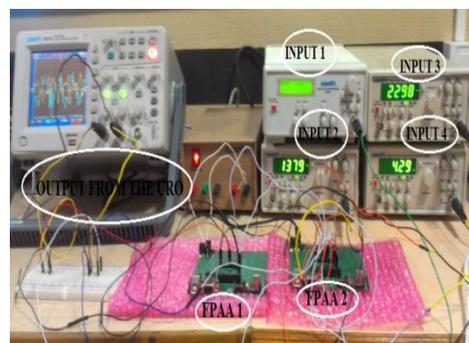

Figure 9. Experimental set-up for testing customized processor using standard input signals.

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(a)   (b)
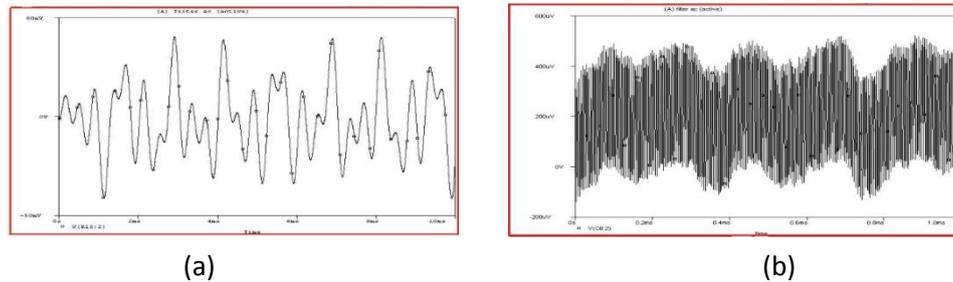
Figure 10. (a) Simulation result for 20 Hz – 4.2 kHz, (b) simulation result of analog processor above 20 kHz.

Figure 10. shows the simulation result of analog processor obtained from Orcad P-spice for the input signal of 200 Hz - 4.2 kHz, and compares the result for two different frequencies. The corner frequencies are 0.616 kHz, 1.380 kHz, 2.29 kHz, and 3.46 kHz for filter 1 to filter 4 respectively and the gain is considered as 4 for all the filters. Figure 10 (a) shows the output of analog processor having the frequencies up to 3.2 kHz without noise signal. Figure 10 (b) shows the output of analog processor having a frequency range beyond 20 kHz has noise signal because the frequency range exceeds the design frequency.

Figure11. shows the audiogram of three case studies with real data of three different patients with HL and compensated output using ASIC implementation.

Case1: Figure 11(a) shows the audiogram of patient having HL at 2 kHz. This patient has HL of 30 dB sensitivity at 2 kHz and more sensitivity at 3 kHz. These losses can be corrected by adjusting the gain factor of that particular band of filter. For 30 dB the gain factor of 31.6 has been set at 2nd band filter and for 15 dB the gain factor of 5.6 has been set for 3rd band filter bank to bring back the sensitivity to 20 dB of normal hearing.

Case2: Figure 12(b) shows the audiogram of patient having HL at 4 kHz. The patient has high sensitive at 1 kHz, 35 dB loss at 4 kHz is corrected by decreasing the gain by factor 5.6 at 2nd filter bank and 35 dB HL is corrected by increasing the gain by factor 56 at 4th filter bank.

Case3: Figure 12(c) shows the audiogram of patient having HL at 2 and 4 kHz. To restore to normal hearing at these HL profile the following compensation are made. 11 dB and 17 dB are considered as more which occurs at 1 kHz and 3 kHz respectively. 11 dB HL can be corrected by decreasing the gain by factor 3 at 1st filter bank, 17 dB loss can be corrected by decreasing the gain by factor 7.07 at 3rd filter bank. Hearing impairment of 35 dB can be corrected by increasing the gain by factor to 56 at 2nd and 4th filter bank.
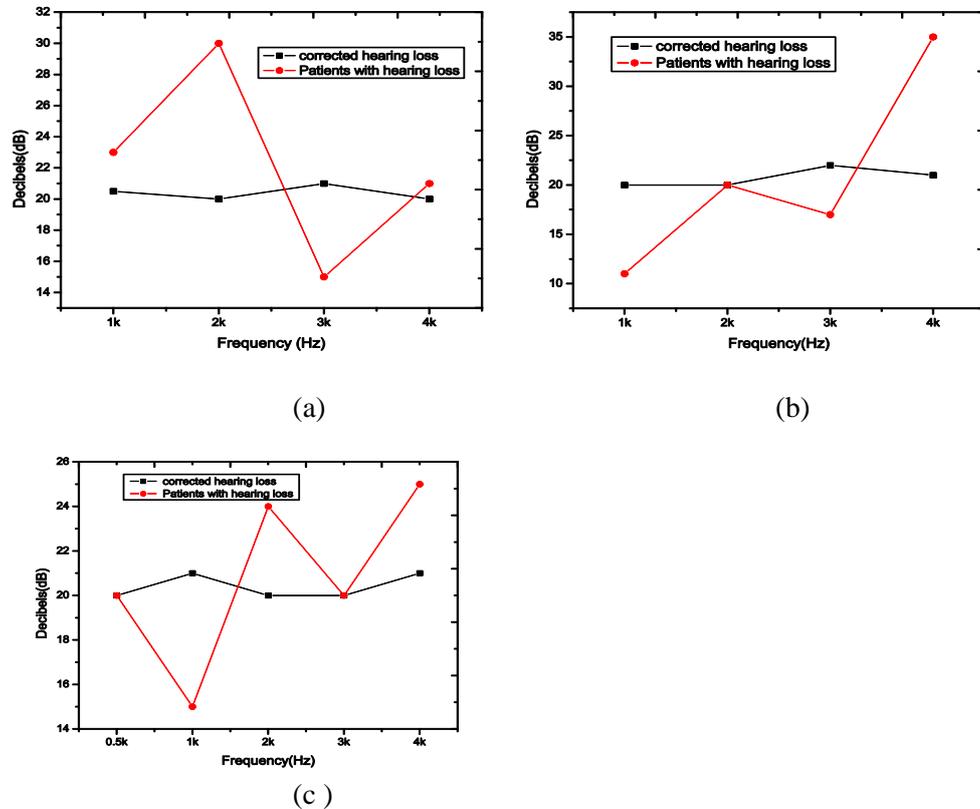
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Figure 12. (a) Audiogram result of case 1, (b) Audiogram result of case 2, (c) Audiogram result of case 3.

5 CONCLUSION

This paper presented the design and implementation of programmable analog hearing aid using FPAA. The advantage of this ASIC processor is easy implementation and cost effective than the digital design. Programmable hearing aid can be configured according to the needs of the individual patient hearing impairment. Four bands of filter has been designed and tested in P-spice and Anadigm designer2 environment. This circuit is analyzed with the standard test input signal and analyzed with and without noise signal. This process is also tested with the real time data obtained from the patients. This proposed methodology can be easily implemented in real application results in manufacturing low cost hearing aid. Further this design can also be implemented with more number of filter bands to achieve precise HL correction.

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REFERENCES

1. Aage R. Moller., "Hearing: Anatomy, Physiology and Disorders of the Auditory System", Academic Press, 2 editions, September 11, 2006.

2. T. B. Deng., "Three-channel variable filter-bank for digital hearing aids" IEEE Transaction on Signal Processing, 4(2), 2010, pp. 181 – 196.

3. Chowdhury, Sazzadur., "Microelectromechanical (MEMS) VLSI structures for hearing instruments." (2000).Electronic Theses and Dissertations, Paper 2728.

4. Yu-Ting Kuo, Tay-Jyi Lin Yueh-Tai Li and Chih-Wei Liu, "Design and Implementation of Low-Power ANSI S1.11 Filter Bank for Digital Hearing Aids", IEEE Transactions on Circuits and Systems I: Regular Papers, 57(7), 2010, pp. 1684 – 1696.

5. B. Hamida, "An Adjustable Filter-Bank based Algorithm for Hearing Aid Systems", Proc. IEEE IECON.99, 3(1999), pp. 1187-1192.

6. S.M. Potirakis and J.Deli, Rangoussi, M., "Steady State and Transient Evaluation of FPAA Implemented Analog Filter using a MLS System Analyzer", IEEE International Conference on Systems, Signals and Image Processing, 2009, IWSSIP 2009, pp.1-8.

7. Joachim Becker and Fabian Henrici, "A Field- Programmable Analog Array of 55 digitally Tunable OTAs in a Hexagonal Lattice", IEEE journal of Solid-State Circuits, 2008, pp. 2759-2760.

8. Kumar, M., Green, E.; De, A.; Roy, S.; Bhattacharya, S., "Field Programmable Analog Array (FPAA) based Shunt Active Filter controller," 2012 IEEE International conference on Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 1011 – 1016.

9. Cioc,, Talpalariu, C.; Talpalariu, J., Matei, C.; Lita, I.; Visan, D.A., "Implementation of charge sensitive amplifier/discriminator for PIN diode radiation detectors",36th International Spring Seminar on Electronics Technology (ISSE), Alba Iulia, 2013, pp. 388 – 392.

10. Ron Mancini, "Op Amps for Everyone", Texas Instruments, 2nd edition, chapter no. 16, 2003, pp. 315-316.