

A Topology for Voltage Source Multilevel Inverter With Lower Number of Switches

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Abstract:- In this study, a novel topology for symmetrical voltage source multilevel inverter is proposed, which comprises series connection of basic unit cells with H-bridge. It offers same voltage level with lower number of power semiconductor switches as compared with traditional cascaded H-bridge and other recent topologies, thereby reducing the number of gate drivers which in turn reduce the installation area and cost of the inverter circuit. In addition, the proposed topology offers fewer number of on-state switches that lead to a reduction in power loss. The operation and performance of the proposed multilevel inverter for 9-level and 15-level is verified through simulation and validated experimentally on a laboratory prototype using dSPACE real-time controller.

Keywords: Voltage source multilevel inverter (VS-MLI), modified SPWM, basic unit cells, reduction of circuit switches.

1. Introduction

In the past few years, voltage source multilevel inverters (VS-MLI) play a vital role for medium and high voltage applications [1], [2]. VS-MLI consists of multiple isolated DC voltage source obtained from diode bridge rectifier or renewable energy sources, and power semiconductor switches to generate a staircase output voltage waveform. The advantages of VS-MLI over classical two-level inverter, has high quality output voltage waveform with less total harmonic distortion (THD), reduced voltage stress on switches and better electromagnetic interference [3], [4].

In general, there are three types of topologies for VS-MLI: flying capacitor inverters, diode clamped and cascaded H-bridge (CHB) [1],[5]-[7]. The above-addressed topologies for VS-MLI have their own advantages and disadvantages [1],[5]-[11]. But the common problem is that as the number of output voltage levels increases, required power semiconductor switches counts increases significantly. It will result in excessive cost and intricacy of switching control scheme, which reduce the efficiency and reliability of inverter. Therefore, many researchers are working towards reducing the circuit components of VS-MLI topologies as follows.

The topology presented in [12] known as semi-cascaded MLI has an advantage of having lower number of power switches over conventional CHB-MLI. But, this inverter suffers from higher peak-inverse-voltage (PIV). Another semi-cascaded MLI introduced in [13], is applicable for both symmetric and asymmetric structure. Comparatively the total PIV and the number of power semiconductor devices are reduced as to semi-cascaded MLI [12]. A symmetric cross connected source (CCS) MLI is available in the literature [14], which has decreased the total PIV compared to that of [13]. Recently, a new structure of MLI has been proposed in [15]. This MLI has a fewer number of switches and total losses are reduced as compared to CMLI inverter. Recently, another semi-cascaded MLI has been proposed [16] with lower power losses and reduced total PIV as compared to that of [12], [13]. Finally a cascaded cross-switch MLI is suggested in [17] is a better choice among all other topologies discussed above [12]-[16]. However, symmetric multilevel voltage source inverter reported in [18] reduced the switches compared to that of [17]. In this research work, a

modified topology is proposed based on symmetric multilevel voltage source inverter, which is reported in literature [18].

Several modulation schemes have been introduced for VS-MLI, such as sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM) and selective harmonic elimination scheme to improve THD and quality voltage waveform [19]-[23]. In this paper, an advanced configuration for VS-MLI has been proposed using universal switching scheme based on SPWM [24-25] is used.

This paper deals with, a new modular configuration for VS-MLI is proposed in which the series connection of basic unit cell will operate with H-bridge inverter in a relevant pattern. This inverter can generate high voltage level with significantly reduced the number of power semiconductor switches needed as compared to the traditional CHB inverter and other recent topologies in [12]-[18]. The proposed topology gives better THD profile in output voltage with proposed modulation scheme. Finally, the simulation and experimental results are analyzed and verified of proposed topology of VS-MLI with universal switching scheme.

2. Proposed topology

The generalized structure of proposed topology consists of series connection of p -basic units, single H-bridge and n -isolated DC sources (including three isolated DC sources of p -basic unit) as depicted in Figure 1. The equivalent circuit of a basic unit cell for proposed topology shown in Figure 2(a). It consists of three DC sources and four power electronics switches. As seen from circuit, switches (S1 and S1') or (S2 and S2') cannot be turned on simultaneously to avoid the short circuit, but they operate in complementary manner. Each basic unit cell can generate four voltage steps including zero and positive level illustrated in Figure 2 (b)-(e). The switching states of the basic unit for four voltage levels are given in Table 1. In this Table, 1 indicates that the relevant switch is on, and 0 indicates the switch is off.

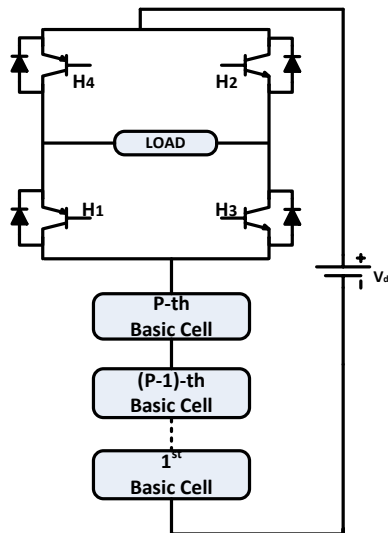


Figure.1 Generalized structure for proposed topology

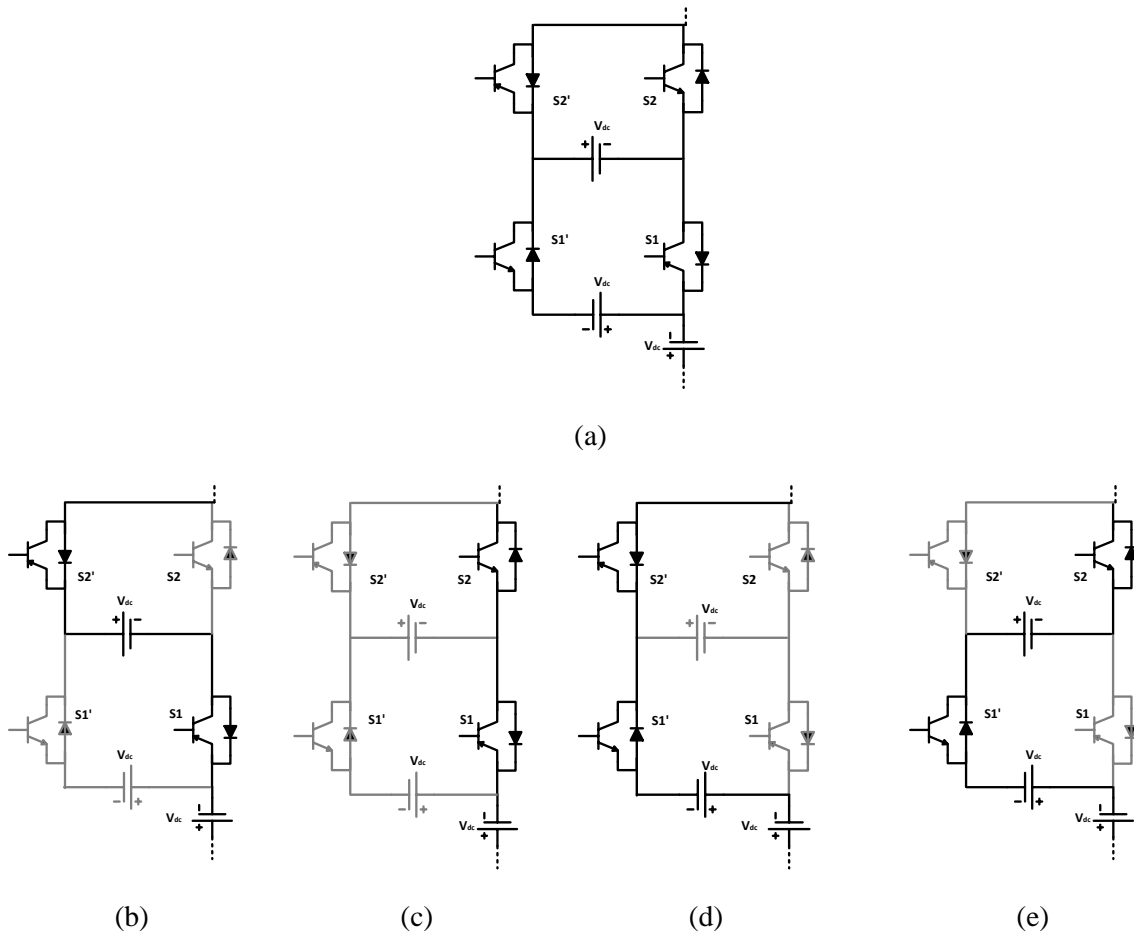


Figure. 2 (a)Equivalent circuit of basic unit cell, and operating state for four different voltage levels
(b) zero level (c) V_{dc} (d) $2V_{dc}$ (e) $3V_{dc}$

Table 1

Switching state for four different voltage levels of basic unit cell

| State | S1 | S2 | Voltage level |
|-------|----|----|---------------|
| 1 | 1 | 0 | 0 |
| 2 | 1 | 1 | $+V_{dc}$ |
| 3 | 0 | 0 | $+2V_{dc}$ |
| 4 | 0 | 1 | $+3V_{dc}$ |

Since each basic unit consists of three DC voltage sources, so with n number of DC sources and p basic unit, the relationship between n and p obtained as follows

$$n = 3p + 1 \tag{1}$$

The basic units are used to generate higher voltage levels in suggested topology but it cannot be able to generate all voltage levels. All voltage levels including positive, negative and zero levels can be obtained with proper switching of H-bridge inverter. The total number of unidirectional switches (N_{switch}) requires in the proposed topology is given by

$$N_{switch} = (n+2) * (4/3) \quad (2)$$

The maximum output voltage of proposed topology can be determined by the following expression

$$(V_{o,max}) = V_{dc} \sum_{i=1}^n i = nV_{dc} \quad (3)$$

The number of output voltage level m is given by the following equation

$$m = 2n + 1 \quad (4)$$

An essential problem in multilevel inverter is the determination of PIV of circuit switches. The total peak inverse voltage (PIV) of circuit switches is calculated as follows .

$$PIV = \sum_{j=1}^{N_{switch}} PIV_{switch_j} \quad (5)$$

Every switch offers an unwanted voltage drop that known as power loss of the switch occurring while switch is changing between on and off state and also during conduction. Therefore, only conduction and switching losses are considered. In the proposed topology, to provide any voltage in the output, half of the switches must be in on state and conduct. To determine the maximum output voltage, the amplitude of the voltage drop in ON state of a switch is assumed to (V_{dp}). Then the following equation (6) is used to determine the maximum output voltage when power losses are considered.

$$(V_{o,max}) = V_{dc} \sum_{i=1}^n i - \left\{ \frac{N_{switch}}{2} V_{dp} \right\} \quad (6)$$

3. Modulation scheme

The schematic diagram of the switching technique is depicted in Figure 3 and the corresponding signals are shown in Figure 4. Eight carriers wave of 1 kHz frequency are employed as carrier signals. Carrier signals are arranged in level shift alternate phase opposition disposition (LS-APOD) SPWM [26]. A sinewave of 50-Hz frequency is as the reference signal. Carrier signals over the time-axis are nominated as $C_s(+t)$, and those below the time axis are nominated as $C_s(-t)$ where, ($s = 1,2,..$). A continuous comparison of the carrier signal with reference signals is carried out. Generated signals from the comparator are summed so as to obtain an aggregated signal 'a(t)' that acquires the same wave shape as that of the expected output voltage level waveform. The switching signals are obtained from aggregated signal by comparing with the desired level signal, and are applied to the circuit switches using look-up table as depicted in Table 2.

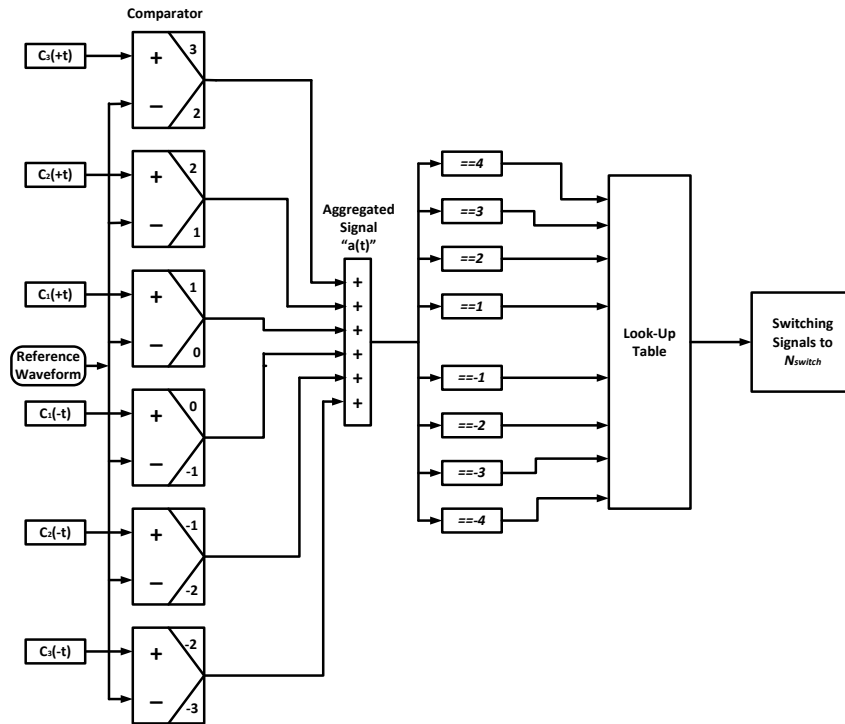
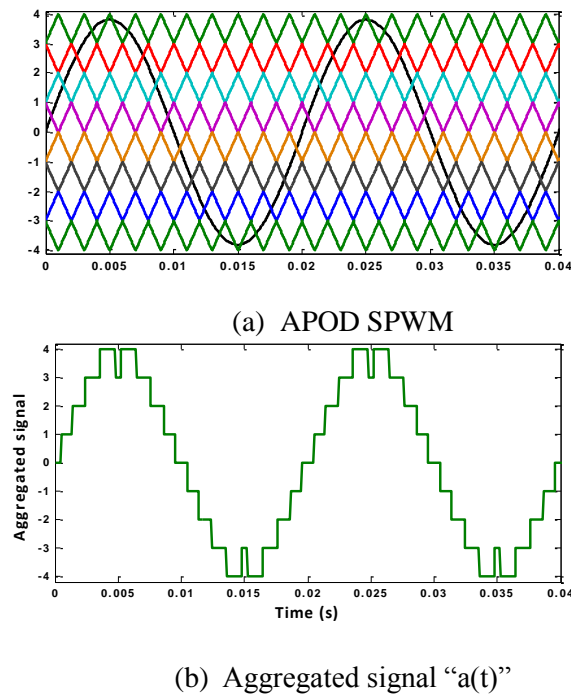
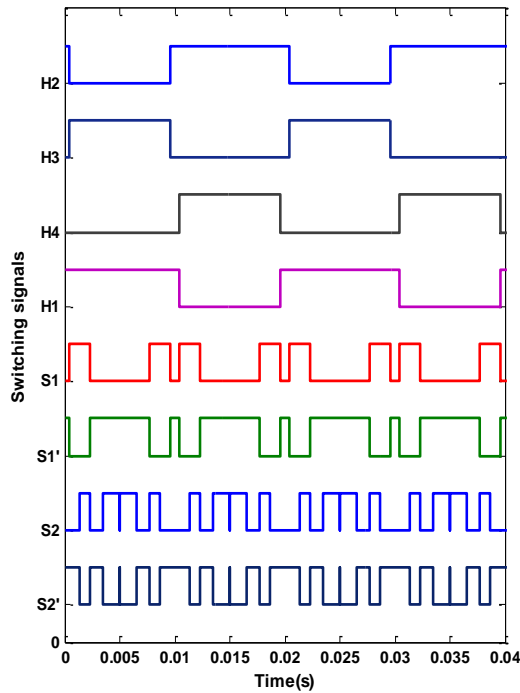
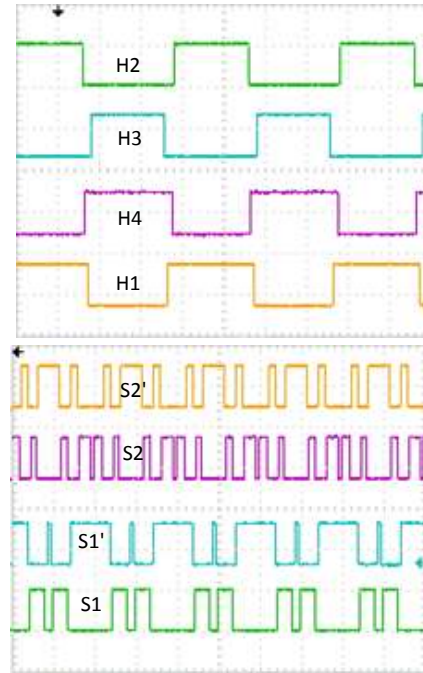


Figure. 3 Block diagram of proposed modulation scheme





(c) Simulated gate signals



(d) Experimental gate signals

Figure. 4 Proposed switching scheme for nine-level inverter

4. Calculation of power losses

There are two types of losses in power electronics converter known as conduction loss and switching loss. Conduction losses are due to on-state resistance and the on-state voltage drop of power switches and the switching losses are due to a non-ideal operation of power switches. In the proposed topology total switches count and on-state switches are lower than the mentioned [12-18] and traditional topology. The calculation of power losses are as follows.

4.1. Conduction losses

Conduction losses for a power switch with the antiparallel diode is estimated and then applied to the proposed inverter. The instantaneous conduction losses for a MOSFET ($P_{c,S}(t)$) and diode ($P_{c,D}(t)$) can be expressed as follows [10].

$$P_{c,S}(t) = [\{ V_T + R_T i^\beta(t) \} i(t)] \quad (7)$$

$$P_{c,D}(t) = [\{ V_D + R_D i(t) \} i(t)] \quad (8)$$

Where, V_T and R_T are on-state voltage and the equivalent resistance of MOSFET, respectively. β is a constant dependent on MOSFET parameters. V_D and R_D are indicated to on-state voltage and resistance of the diode, respectively.

To calculate the total conduction loss, it is required to define the switches count, $N_S(t)$, and diodes, $N_D(t)$, existing in the current path. It is noticeable that, output voltage level and operating conditions (in the current direction) affect the quantity of on-state switches that is time-variant. The average conduction losses are written as follows:

$$P_c = \frac{1}{\pi} \int_0^\pi [\{N_S(t) \times P_{c,s}(t)\} + \{N_D(t) \times P_{c,D}(t)\}] d(\omega t) \quad (9)$$

4.2 Switching Losses

To calculate the total switching loss of the proposed inverter, the energy loss during on and off-state of a typical power switch with the body diode is considered first and then that amount is applied to the proposed inverter. Suppose that the voltage and current varies linearly during on and off time a switch can be expressed as follows.

$$E_{on} = \int_0^{t_{on}} v(t) i(t) dt$$

$$= \int_0^{t_{on}} \left[\left(\frac{V_{sw}}{t_{on}} t \right) \left(-\frac{I}{t_{on}} (t - t_{on}) \right) \right] dt = \frac{1}{6} V_{sw} I t_{on} \quad (10)$$

$$E_{off} = \int_0^{t_{off}} v(t) i(t) dt$$

$$\int_0^{t_{off}} \left[\left(\frac{V_{sw}}{t_{off}} t \right) \left(-\frac{I}{t_{off}} (t - t_{off}) \right) \right] dt = \frac{1}{6} V_{sw} I t_{off} \quad (11)$$

where E_{on} and E_{off} are on-state and off-state loss energy and t_{on} and t_{off} are the on and off-state period of the switch respectively. I is the current through the switch and V_{sw} is voltage across the switch before turned-off or turned-on. The total switching loss can be obtained as follows.

$$P_{sw} = f(N_{on}E_{on} + N_{off}E_{off}) \quad (12)$$

where f , is the fundamental frequency. N_{on} is the number of on-states and N_{off} is the number of off-states. The total power losses of proposed inverter can be obtained using (12) and (15) as

$$\text{Total power losses, } (P_{Loss}) = P_c + P_{sw} \quad (13)$$

In this study, following parameters are considered to determine the power loss of proposed topology:

$R_T = 0.25$ Ohm, $R_D = 0.11$ Ohm, $V_T = 2.5V$, $V_D = 1.2V$, $\beta = 1$, $t_{on} = t_{off} = 1$ μ sec. $f = 50$ Hz. Each isolated DC voltage source has magnitude 12V. The load resistance is 15 Ohm. The mathematical calculation is carried out for each Switch (MOSFET) for one cycle using equations (7) to (13) and total power loss for one second is obtained 2.452 mW.

5. Simulation results

Simulation studies of the proposed topology are presented to verify the performance. The simulation has been carried out in MATLAB/Simulink ver. 7.8 running on a computer (core i7-4770, 3.40 GHz, 2 GB RAM), the simulation studies are as follows.

5.1.Nine-level inverter

The equivalent circuit of nine level inverter of proposed topology is shown in Figure 5, the circuit consists eight unidirectional switches and four DC sources with the magnitude of 12V each (including basic unit cell indicated in dashed area), which produce the staircase voltage waveform of maximum output 48V. In practical, required number of dc source can be easily obtained in application such as solar cells, fuel cells and AC drives, where multi-winding transformer are often employed and thus separate DC sources are obtained by rectification of secondary voltages. A series R-L branch ($R = 15$ Ohm and $L = 20$ mH) is considered as load parameters. The waveforms of output voltage and load

current of the nine-level inverter are shown in Figure 6(a), and harmonic spectrum of the output voltage is shown in Figure 6(b). The look-up table for switching states is given in Table 2.

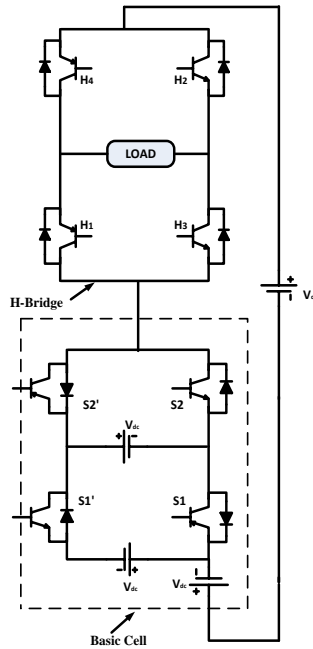
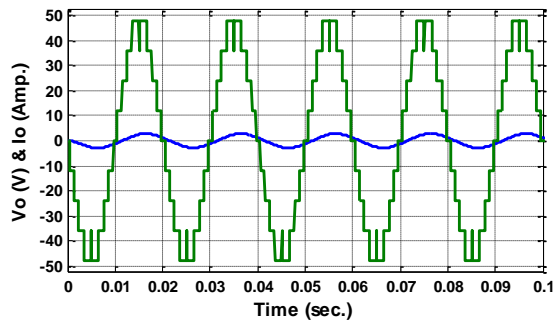
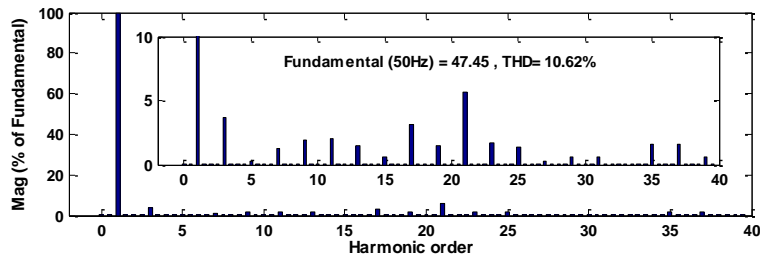


Figure 5 Equivalent circuit of nine-level inverter for proposed topology



(a) Nine-level output voltage and current waveform



(b) Harmonic spectrum of output voltage

Figure 6 Waveforms corresponding to simulation results for 9-level inverter

Table 2

Look-up table for switching state for 9-level inverter of proposed topology

| State | Aggregated signal "a(t)" | Output voltage | ON state switches |
|-------|--------------------------|----------------|--------------------|
| 1 | 4 | $4V_{dc}$ | $S1', S2, H1, H2$ |
| 2 | 3 | $3V_{dc}$ | $S1', S2', H1, H2$ |
| 3 | 2 | $2V_{dc}$ | $S1, S2, H1, H2$ |
| 4 | 1 | V_{dc} | $S1, S2', H1, H2$ |
| 5 | 0 | 0 | $H1, H3/H2, H4$ |
| 6 | -1 | $-V_{dc}$ | $S1, S2', H3, H4$ |
| 7 | -2 | $-2V_{dc}$ | $S1, S2, H3, H4$ |
| 8 | -3 | $-3V_{dc}$ | $S1', S2', H3, H4$ |
| 9 | -4 | $-4V_{dc}$ | $S1', S2, H3, H4$ |

5.2. Fifteen-level inverter

To validate this fact that the proposed topology can generate more voltage level, the equivalent circuit of the fifteen-level inverter is shown in Figure 7. The circuit consists of seven DC sources with the magnitude of 12V each and twelve unidirectional switches (including the two basic unit cell indicated in dashed area), which produce the staircase voltage waveform of maximum output 84V. The voltage and current waveforms of the fifteen-level inverter are shown in Figure. 7(a), and harmonic spectrum of the output voltage has significant THD of 7.86% as shown in Figure 10(b). The look-up table for switching states is given in Table 3

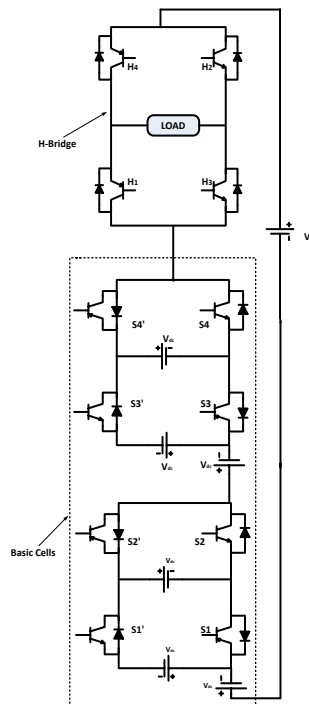
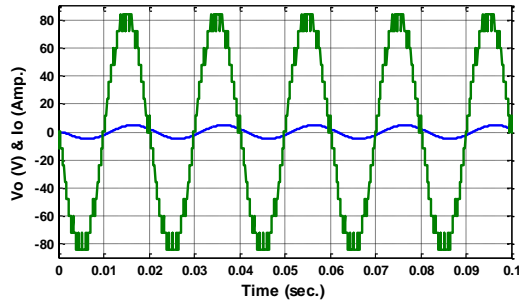
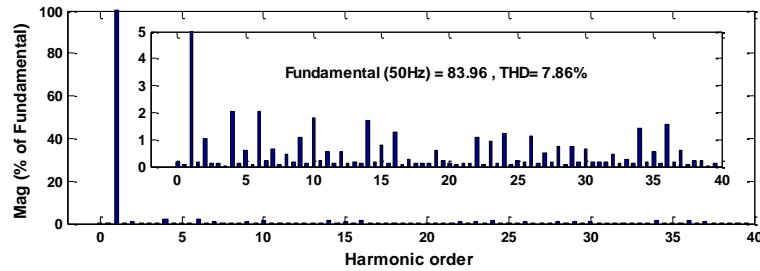


Figure 7 Equivalent circuit of fifteen-level inverter for proposed topology



(a) Fifteen-level output voltage and current waveform



(b) Harmonic spectrum of 15-level output voltage

Figure 8 Waveforms corresponding to simulation results for 15-level inverter

Table 3

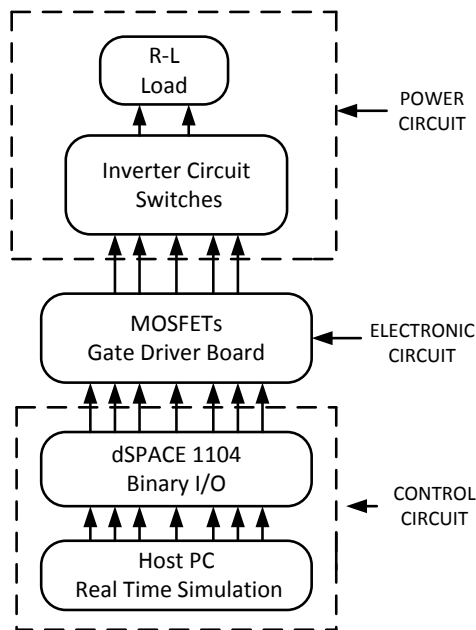
Look-up table for switching state for 15-level inverter of proposed topology

| State | Aggregated signal "a(t)" | Output voltage | ON state switches |
|-------|--------------------------|----------------|------------------------------|
| 1 | 7 | $7V_{dc}$ | $S1', S2, S3', S4, H1, H2$ |
| 2 | 6 | $6V_{dc}$ | $S1', S2, S3', S4', H1, H2$ |
| 3 | 5 | $5V_{dc}$ | $S1', S2', S3', S4', H1, H2$ |
| 4 | 4 | $4V_{dc}$ | $S1', S2', S3, S4, H1, H2$ |
| 5 | 3 | $3V_{dc}$ | $S1, S2, S3, S4, H1, H2$ |
| 6 | 2 | $2V_{dc}$ | $S1, S2', S3, S4, H1, H2$ |
| 7 | 1 | V_{dc} | $S1, S2', S3, S4', H1, H2$ |
| 8 | 0 | 0 | $H1, H3/H2, H4$ |
| 9 | -1 | $-V_{dc}$ | $S1, S2', S3, S4', H3, H4$ |
| 10 | -2 | $-2V_{dc}$ | $S1, S2', S3, S4, H3, H4$ |
| 11 | -3 | $-3V_{dc}$ | $S1, S2, S3, S4, H3, H4$ |
| 12 | -4 | $-4V_{dc}$ | $S1', S2', S3, S4, H3, H4$ |
| 13 | -5 | $-5V_{dc}$ | $S1', S2', S3', S4', H3, H4$ |
| 14 | -6 | $-6V_{dc}$ | $S1', S2, S3', S4', H3, H4$ |
| 15 | -7 | $-7V_{dc}$ | $S1', S2, S3', S4, H3, H4$ |

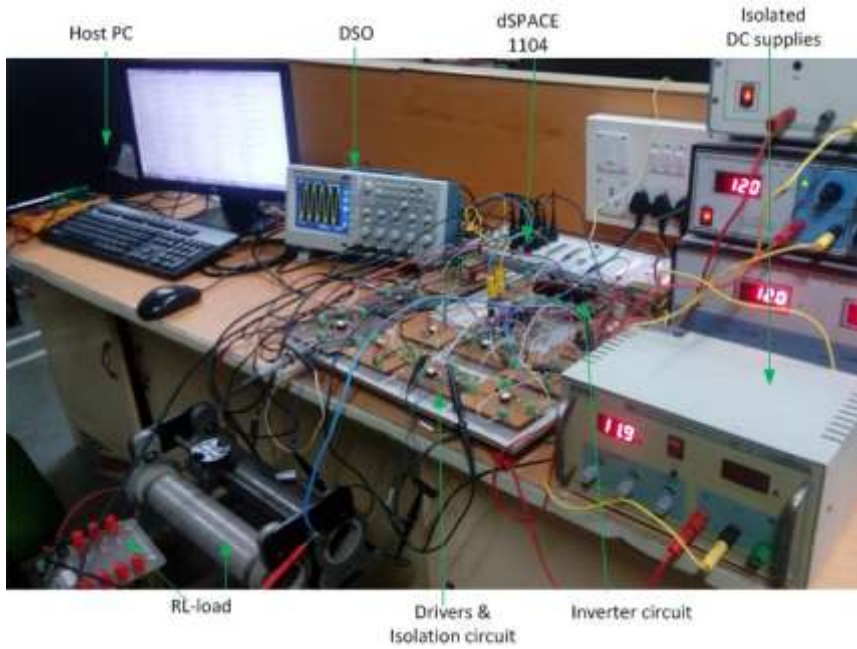
6. Experimental results

To ensure the feasibility of the proposed topology, equivalent circuit of single phase 9-level and 15-level inverter are shown in Figure 5 and Figure 7 respectively, have been implemented in the laboratory. The prototype of 9-level inverter consists of eight MOSFET (IRF 540) switches and four

isolated DC supplies, whereas 15-level inverter consists of twelve MOSFET (IRF 540) switches and seven isolated DC supplies. MOSFETs are driven by MCT2E optocouplers and series R-L branch ($R=15\text{ Ohm}$ and 20mH) considered as AC load. dSPACE DS 1104 real time controller has been used for real-time simulation for switching control design in MATLAB/SIMULINK environment. The developed code of Simulink model of switching algorithm is electronically generated by real time of MATLAB in conjunction with real time interface of dSPACE. The generated C-code is downloaded into DS 1104 and generation of switching pulses for MOSFETs switches shown in Figure 4(d). A schematic diagram of hardware prototype and image of experimental set-up developed in laboratory are shown in Figure 9. The output voltage and load current waveforms of implemented circuit of the nine-level and fifteen-level inverter are shown in Figure 10. The transient response is shown in Figure 11 for a variation in load. It is observed that the change in load current does not affect the output voltage.

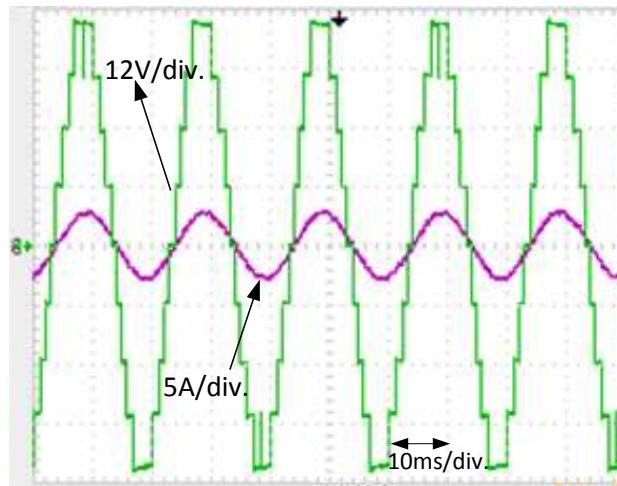


(a) Block diagram of experimental set-up

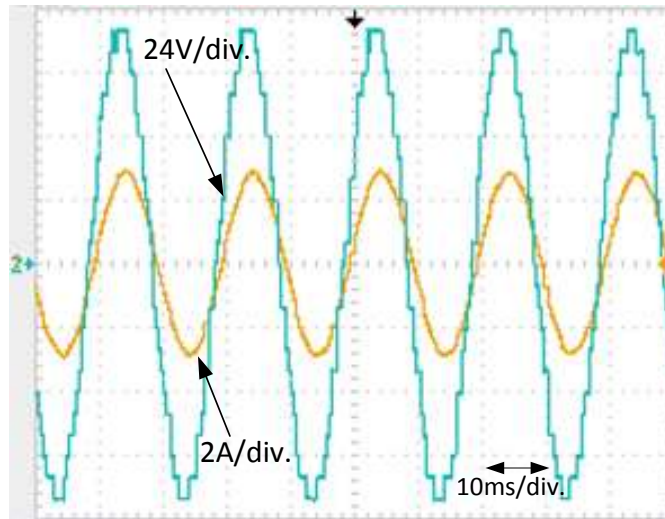


(b) Image of experimental setup

Figure.9 Experimental set-up developed in laboratory



(a) Output voltage and load current for 9-level inverter



(b) Output voltage and load current for 15-level inverter

Figure. 10 Experimental results

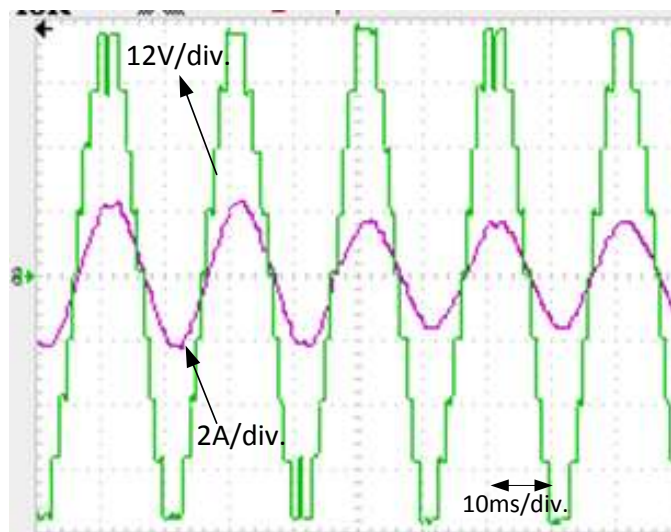


Figure. 11 Transient response of output voltage and load current for 9-level inverter during change in load

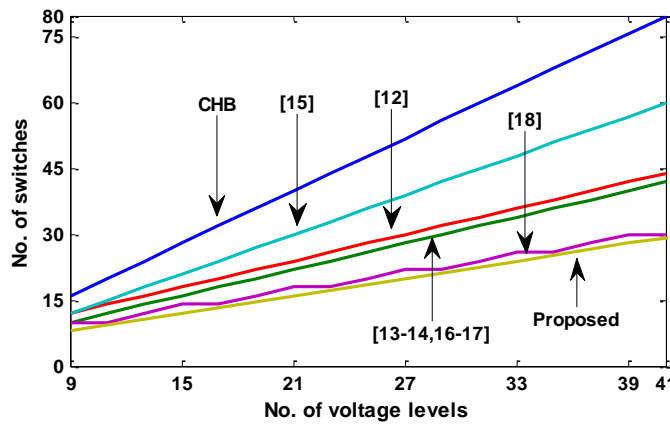
7. Comparative analysis

The main objective of this paper is to present a new structure for symmetrical VS-MLI with required number of power semiconductor switches is lower than the conventional CHB and other recent topologies. The number of power semiconductor switches and rating of them are great attention in VS-MLI. It can be seen from Table 4 that the number of power semiconductor switches in the proposed topology are significantly lower than the traditional CHB and other recent topologies for same voltage levels as shown in Figure 12(a). Table 4 also represents the total PIV of proposed topology is lesser than the mentioned topologies in the literature [12]-[13], [16] and same as with the same number of DC voltage sources.

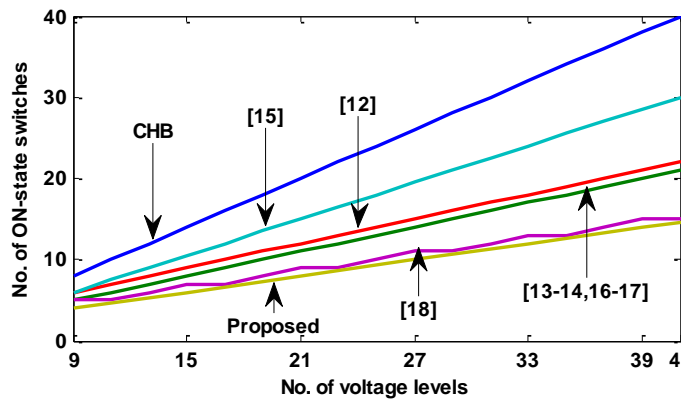
Table 4

Comparison of different multilevel inverter topologies

| Type of topology | Number of switches | PIV (pu.) |
|-------------------------|--------------------|-----------|
| <i>Conventional CHB</i> | $4n$ | $4n$ |
| <i>Ref. [12]</i> | $2(n+2)$ | $6n$ |
| <i>Ref. [13]</i> | $2(n+1)$ | $2(3n-1)$ |
| <i>Ref. [14]</i> | $2(n+1)$ | $4n$ |
| <i>Ref. [15]</i> | $3n$ | $4n$ |
| <i>Ref. [16]</i> | $2(n+1)$ | $2(3n-2)$ |
| <i>Ref. [17]</i> | $2(n+1)$ | $4n$ |
| <i>Ref. [18]</i> | $(4n+14)/3$ | $2(3n-1)$ |
| <i>Proposed</i> | $(n+2)(4/3)$ | $2(3n-1)$ |



(a) Number of power switches against number of voltage levels



(b) Number of on-state switches against number of voltage levels

Figure. 12 Comparison of proposed topology with other topologies

The on-state switches in multilevel inverter lead to undesired voltage drop that causes the power loss. The number of on-state switches is lower in the proposed topology in contrast to contemporary topologies as shown in Figure 12(b). Therefore, the total power loss of the proposed topology is reduced, and improves the efficiency of the inverter.

8. Conclusion

In this paper, a novel topology for symmetrical voltage source multilevel inverter has been proposed, with the objective of using lower number of switches and related gate drivers realizing the same output voltage level compared with conventional CHB and recent topologies. The comparison analysis shows that the total PIV and power loss of the proposed topology are fewer than the mentioned topologies for voltage source multilevel inverter. Additionally, it offers advantages such as, reduction in size, cost effective and has simple control switching scheme. Simulation and experimental results validate the performance of proposed topology for symmetric multilevel inverter.

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