

Modified Bridgeless Rectifier for PFC with Minimized Stress

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Abstract. A high performance single phase modified bridgeless ac-dc converter with an automatic power factor correction is introduced. The proposed converter is based on a single ended primary inductance converter (SEPIC) topology and operated in continuous conduction mode (CCM) to meet the demands of power factor correction (PFC) to unity and output voltage regulation. It offers many advantages, such as fewer semiconductor devices, low stress on each component, improved efficiency, high power factor compared to classical converter. Detailed analysis of the converter is presented. Simulation and experimental results are discussed for a 300W prototype to verify the performance of the converter.

Keywords: Power factor correction (PFC); continuous conduction mode (CCM); single ended primary inductance converter (SEPIC).

1. Introduction

Many applications like computers, telecom equipment, biomedical industries and LED lighting uses AC-DC conversion which involves conventional bridge rectifier with large capacitor at output end is unavoidable, results in low power factor of about 0.5-0.7[1]. As per the Stringent international standards like International Electronic Commission (IEC) 6100-3-2, harmonics produced by the electronic equipment like rectifiers should be limited [2]. Therefore, the power factor improvement is mandatory for single phase power supplies to meet the demands like reduction of current harmonics and power factor correction (PFC). The most conventional PFC converter is a bridge rectifier followed by a DC-DC converter. Boost converter is widely used as the DC-DC converter in PFC circuits because of its simplicity, low cost and high performance though it is having output voltage greater than the peak input voltage.

In large no of applications, it is preferred to have the PFC output voltage lower than the input ac voltage, a buck type converter is recommended. The input current of buck converter is discontinuous and to shape it like sinusoidal another passive filter must be used at the input side of the buck converter. This is the characteristics of all converters in which a buck converter is at its input, such as buck-boost, noninverting buck-boost, flyback etc., [3-5]. On the other side, a SEPIC converter can provide a high power factor regardless of its output voltage due to its step up/down function. However, all the above addressed conventional PFC rectifiers includes a front end bridge rectifier which leads to high conduction losses, resulting in additional thermal management and decrease the efficiency of the PFC converter. In order to enhance the efficiency of the conventional PFC

converters bridgeless PFC converters have been proposed such as buck, buck-boost, boost, sepic [6-17]. Since Bridgeless PFC rectifiers has lower no of semiconductor devices in the current path ,results in lower conduction losses ,higher efficiency and cost saving.

The bridgeless PFC boost rectifier is predominant because of its simplicity but it has same major practical drawbacks like difficulty in providing input-output isolation, high startup inrush current and lack of current limiting during overload conditions as in conventional boost PFC converter. Therefore research has been focused on bridgeless sepic PFC since it is a solution for many applications. Recently many bridgeless SEPIC PFC converters have been proposed in the literature. Bridgeless SEPIC PFC circuits that are proposed in the literature [18-23], operates under DCM mode suffers with high voltage and current stress that highly degrades the performance of the converter and limits its application range.

To overcome aforementioned defects, a modified bridgeless SEPIC PFC with continuous conduction mode (CCM) with reduced stress is presented. This meets the challenges of near unity power factor and output voltage regulation. The remaining sections of the paper is organized as follows. Principle of operation is discussed in section 2. In section 3 theoretical analysis are design procedure and experimental considerations are given. Efficiency improvement is explained in section 4. The simulation results are presented in section 5. Experimental results and conclusion are given in section 6 and 7, respectively.

2. Operation of Bridgeless SEPIC converter in CCM mode

The circuit diagram of conventional SEPIC PFC rectifier and modified Bridgeless SEPIC are shown in Fig.1 and Fig.2. Bridgeless SEPIC is combination of both bridge rectifier and classical SEPIC converter, so it is known as Bridgeless SEPIC converter. It is having fewer semiconductor components. Operation of the circuit is similar to classical sepic converter and is symmetrical in two half –line cycles of input voltage. Thus, the operation of the converter is considered during one switching period in the positive half –line cycle of the input voltage. The converter is operated in CCM mode i.e., output diode turns off when the switch is turned on. The capacitance of the output capacitor C_o is adequately high enough to make it ideal dc voltage source as shown in Fig.2. Also, the supply voltage is assumed constant and equal to V_{in} in a switching period T_s .

To simplify the analysis, it is assumed that the converter is operating at steady state and all components are ideal. The circuit operation in a switching cycle is divided into two modes. Fig.3 and Fig.4 shows the schematic diagram of mode I and mode II in the positive half cycle. The theoretical waveforms of the converter are shown in Fig.5.

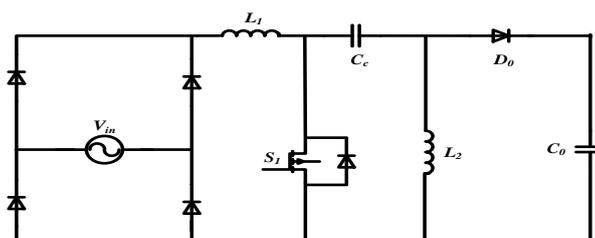


Fig 1. Conventional SEPIC PFC rectifier

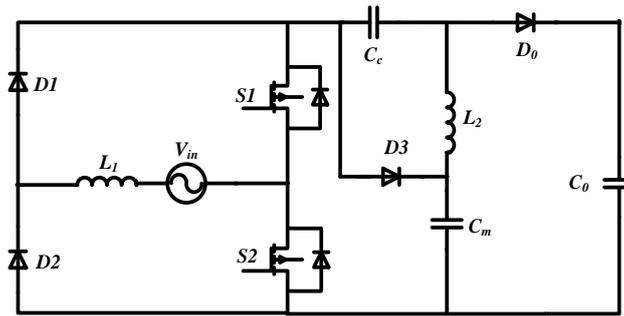


Fig 2. Modified Bridgeless SEPIC PFC rectifier

Mode I (t_0-t_1):

At t_0 , both switches S1, S2 and diode D1 are in ON state and output diode D_0 is in OFF state. Capacitors C_c and C_m follows the input voltage. The load current is provided by the output capacitor as the output diode is reverse biased. Here the switch current is combination of currents flowing through inductors L_1 and L_2 . Input inductor current i_{L1} starts to increase linearly by a slope of $V_{in}(t_0)/L_1$ and output inductor current i_{L2} starts decreasing linearly by the slope of $(V_{Cc} - V_{Cm})t_0/L_2$. This mode ends by turning off the switches S1 and S2. Switch current is given by the equation (1).

$$I_{S1(t)} = i_{L1} - i_{L2} = \left(\frac{V_{in}(t_0)}{L_1} + \frac{V_{in}(t_0)}{L_2} \right) t \quad (1)$$

$$\text{where } i_{L1} = \left(\frac{V_{in}}{L_1} \right) (t - t_0) \quad (2)$$

$$i_{L2} = \left(\frac{V_{Cc} - V_{Cm}}{L_2} \right) (t - t_0) = \left(\frac{-V_{in}}{L_2} \right) (t - t_0) \quad (3)$$

$$-V_{Cc} + V_{Cm} = V_{in} \quad (4)$$

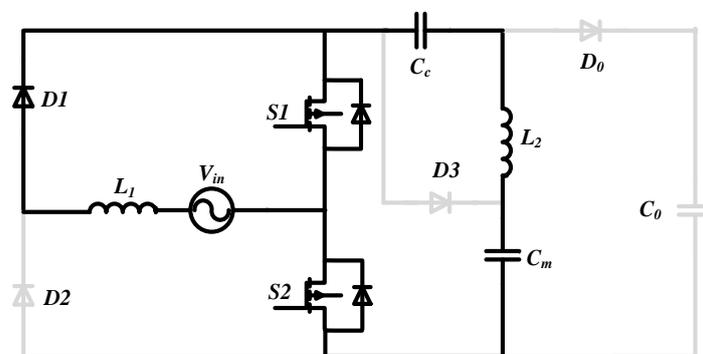


Fig 3. Mode I

Mode II (t_1 - t_2):

At t_1 , switches S1 and S2 are turned off and diodes D3 and D₀ starts conducting. The voltage across switches begins to increase. Energy stored in the input inductor is transferred to the output through the coupling capacitor C_{c1} and output diode D₀ and also to the C_{c2} through diode D₃ at the same time .Energy stored in inductor L2 is transferred to the output through diode D0.This mode ends by starting the next switching cycle at t_2 .

$$i_{L1} = i_{L1}(t_1) + \frac{-V_{Cc} + V_{Cm}}{L_1}(t - t_1) \quad (5)$$

$$i_{L2} = i_{L2}(t_1) + \frac{V_{Cc}}{L_2}(t - t_1) \quad (6)$$

$$V_0 = V_{Cc} + V_{Cm} \quad (7)$$

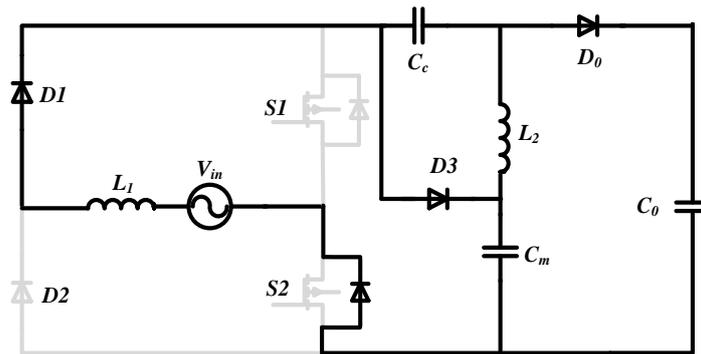


Fig 4. Mode II

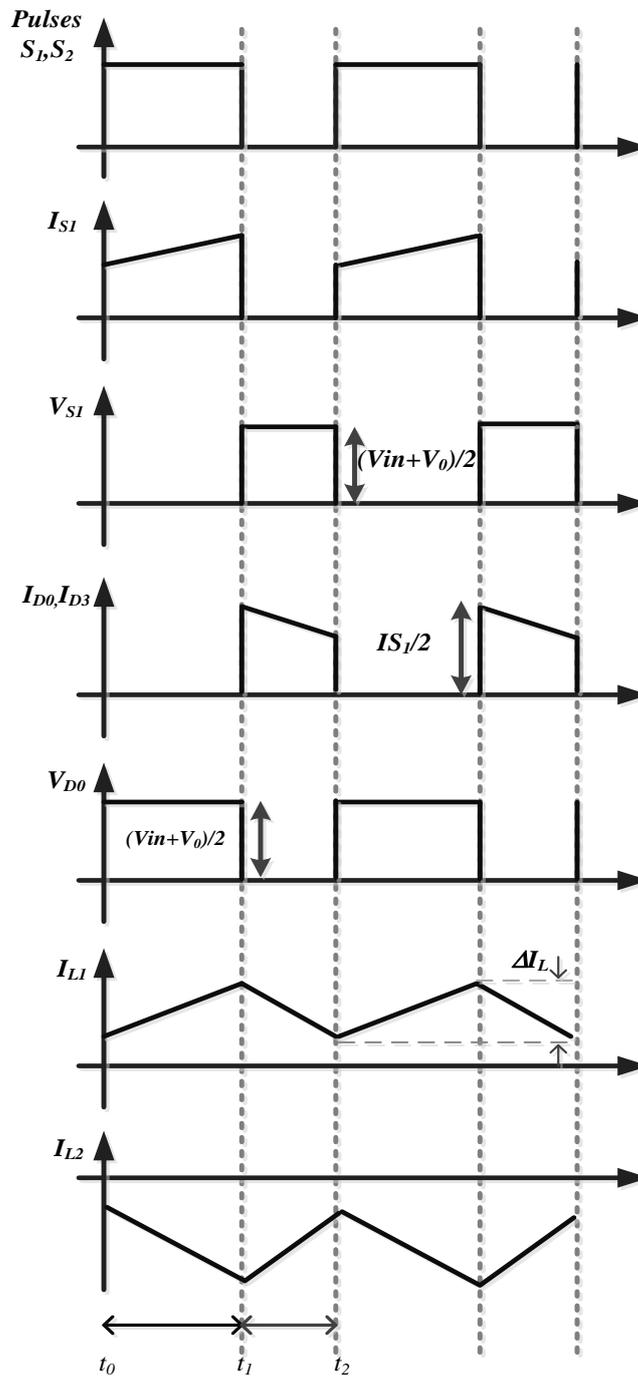


Fig 5. Theoretical waveforms of the Converter

3. Theoretical Analysis

3.1 Static gain:

The average inductor voltage at steady state is considered to be zero. By applying volt-second balance to the inductor L_1 is given by equation (8)

$$V_{in}t_{on} = (-V_{in} + V_{cm})(T - t_{on}) \quad (8)$$

From equation (4) & (7) we get

$$V_{cm} = \frac{V_0 + V_{in}}{2} \quad (9)$$

From equation (8) & (9) we get

$$D = \frac{t_{on}}{T} = \frac{V_0 - V_{in}}{V_0 + V_{in}} \quad (10)$$

Now, static gain is given by equation (11)

$$\frac{V_0}{V_{in}} = \frac{1 + D}{1 - D} \quad (11)$$

3.2 Inductors L_1 and L_2 :

Inductors L_1 and L_2 are calculated as a specification of maximum input current ripple (Δi_L). The peak input current is calculated by equation (12) assuming the current ripple given by equation (13). The inductors L_1 and L_2 are given by equation (14)

$$I_{in(peak)} = \frac{\sqrt{2}P_0}{\eta V_{in(rms)}} \sin(\omega t) \quad (12)$$

$$\Delta i_L = \frac{V_{in} D}{L f_s} \quad (13)$$

$$L_1 = L_2 = \frac{V_{in} D}{\Delta i_L f_s} \quad (15)$$

3.3 Capacitors C_c and C_m

It has a considerable impact in the input current waveform since the capacitors C_c and C_m follows the input line voltage within line period and is constant in one switching period. Resonant frequency (f_r) plays a vital role in the design of capacitor C_c and C_m . The resonant frequency (f_r) of coupling capacitor C_c and C_m , inductor (L_1) and inductor (L_2) should be greater than line frequency (f_l) to avoid the input current oscillations at each half line cycle, likewise resonant frequency (f_r) should be lower than the switching frequency (f_s) to make sure that the capacitor voltage is constant in a switching time (T_s). Accordingly C_c and C_m can be obtained from the following equation.

$$C_m = C_c = \frac{1}{4\pi f_r^2(L_1 + L_2)} \quad (16)$$

Where $f_l < f_r < f_s$

f_r value is chosen as 5 kHz to meet the requirement.

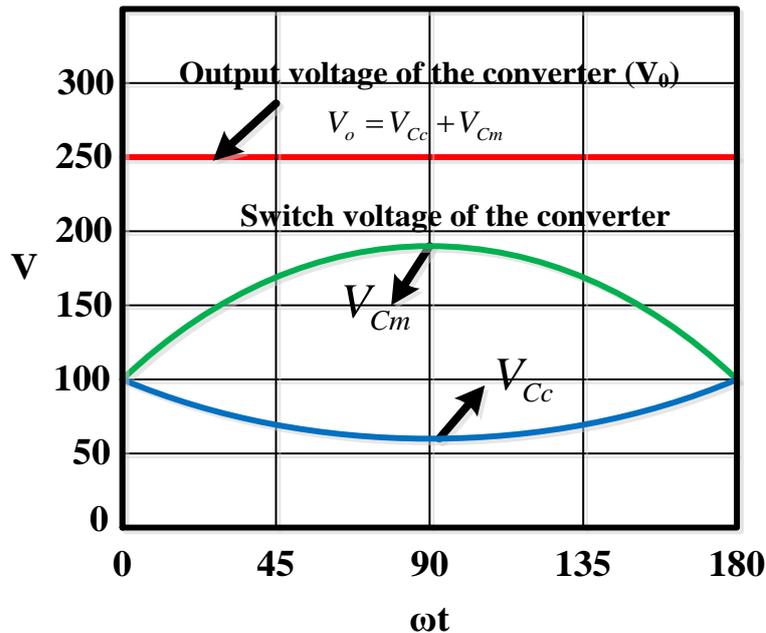


Fig 6. Theoretical waveforms of the Capacitor voltages

The voltage across the capacitors C_c and C_m are given by the equation (17) and (18) and are shown in Fig .6.

$$V_{C_c} = V_{in} \left(\frac{1}{1-D} \right) \quad (17)$$

$$V_{C_m} = V_{in} \left(\frac{D}{1-D} \right) \quad (18)$$

3.4 Output Capacitor C_0

Since output voltage ripple is two times the input line frequency, output capacitor must be large enough to reduce the output voltage ripple ΔV_0 . Therefore, output capacitor voltage is obtained from the following equation

$$C_0 = \frac{P_0}{4f_l V_0 \Delta V_0} \quad (19)$$

where f_l is input line frequency and ΔV_0 is output voltage ripple.

3.5 Maximum voltage and current rating of switching devices

The maximum switch voltage and current of the converter is obtained from the following equation.

$$V_{S1,2(\min)} = \frac{V_{in(\min)} + V_0}{2} \quad (20)$$

$$V_{S1,2(\max)} = \frac{V_{in(\max)} + V_0}{2} \quad (21)$$

$$I_{S1(\min)} = I_{in(\min)} + \Delta I_L + I_0 \quad (22)$$

$$I_{S1(\max)} = I_{in(\max)} + \Delta I_L + I_0 \quad (23)$$

3.6 Controller Design

The average current mode control is used to generate the current reference for the bridgeless SEPIC converter. The design of the converter is done based on CCM mode. The converter uses UC3854 as a controller, which gives current shape and frequency that follows line current using synchronous feedback loop [25].

To get near unity power factor, the controller needs voltage and current feedback signals are sensed from the converter. In the given circuit input voltage is sensed from capacitors C_c and C_m since they follows the input voltage, Input inductor current signal is sensed from diode currents (I_{D1} and I_{D2}) as shown in Fig.7. Then the reference current is computed by a multiplier of the synchronous feedback loop, output voltage feedback loop, and input voltage feed forward loop. The control circuit of the converter is shown in Fig.7. The voltage feedback loop should have a very low bandwidth, well below the line frequency, in order to minimize input current distortion [26,27].

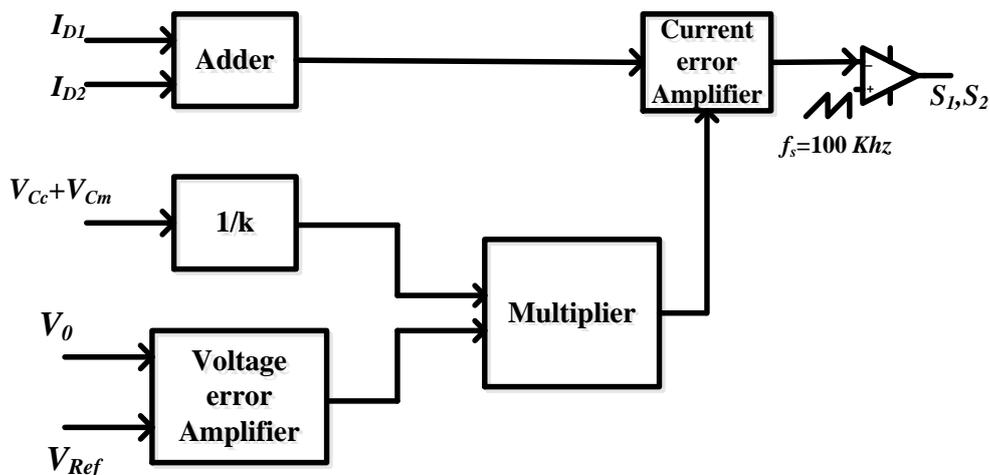


Fig 7. Block diagram for Controller

4. Efficiency improvement

Based on the number of components present in the converter, the efficiency enhancement of the converter is analyzed. From the operation of the converter, it is seen that a diode in the rectifier is removed and the other diode is substituted by a switch. Assuming the forward voltage drop of the diodes in the converter is 1V and the voltage drop of the power MOSFET is negligible since $R_{DS(on)}$ is small. The theoretical calculations of the power dissipation of the reduced components is given by (24).

$$P_{D,avg} = \frac{1}{T} \int_0^T V_D I_D dt = 3.15W \quad (24)$$

Where $T = \pi$, $V_D = 1V$, $I_D = 4.991 \sin(\omega)$ and $P_{D,avg}$ is average power loss in one diode of the input rectifier. The efficiency improvement of 300W converter is calculated by (25).

$$\eta_{improvement} = \frac{2P_{D,avg}}{300} = 2.11\% \quad (25)$$

In general the efficiency enhancement is less than 2.11% due to the assumption of the zero voltage drop of switch.

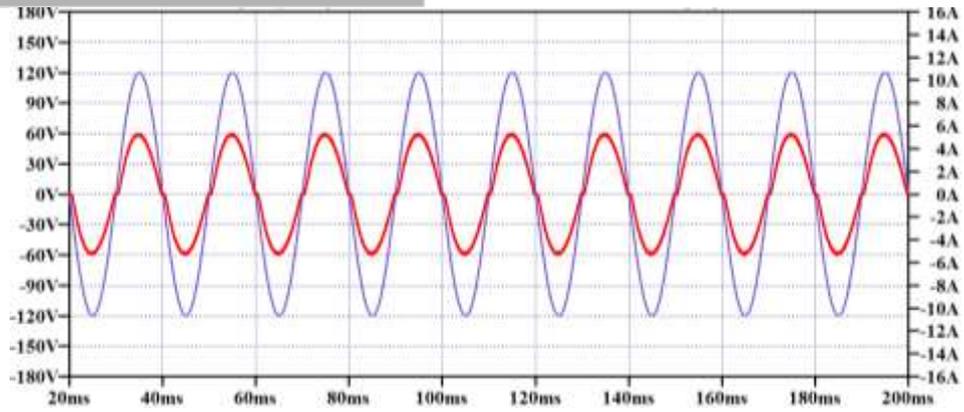
5. Simulation results

The proposed converter is simulated in LT Spice IV. Specifications and parameters of the converter are as follows: $V_{in} = 85 V_{Rms}$, $V_0 = 250 V_{dc}$, $\Delta i_{L1} = 20\%$ of i_{L1} , $f_s = 100$ kHz and $P_0 = 300$ W. According to the design considerations, the circuit elements are obtained as $L_1 = L_2 = 2$ mH, $C_c = 0.62 \mu F$, and $C_0 = 1200 \mu F$.

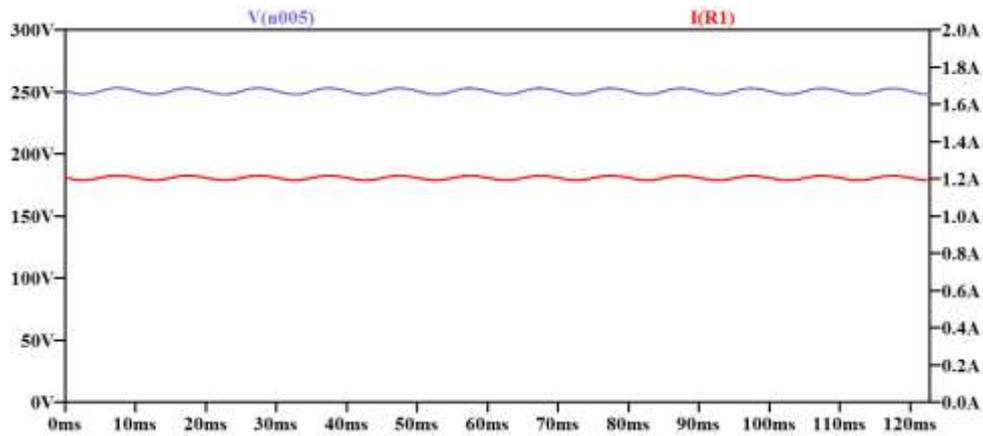
To achieve PFC and regulated output voltage average current mode control is used. It includes an inner current loop and outer voltage loop. Here capacitor voltages are sensed since they follows input voltage which is given to one of the multiplier input. The output voltage is sensed and processed through voltage error amplifier which feeds the other input port of the multiplier. The output of the multiplier generates current reference which is compared with input current that is sensed from sum of the diode current. The output of the current error signal is compared with ramp signal to generate gate pulses.

The input voltage and current waveforms in simulation are shown in Fig. 8 (a). It is observed that both are in phase which depicts the property of power factor correction of the converter. Fig .8 (b) illustrates the output voltage and output current waveforms respectively. The capacitor voltage waveforms and inductor currents are shown in Fig. 9 (a) and Fig .9 (b) and it can be observed that current waveforms of the inductors L_1 and L_2 are continuous which assure converter is operated in CCM mode. Switch current and output diode current waveforms are shown in Fig .9 (c).

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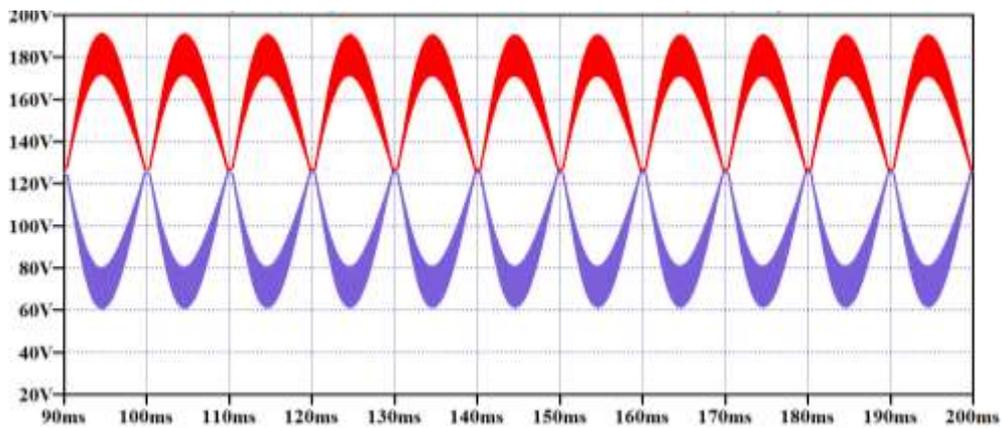


(a)



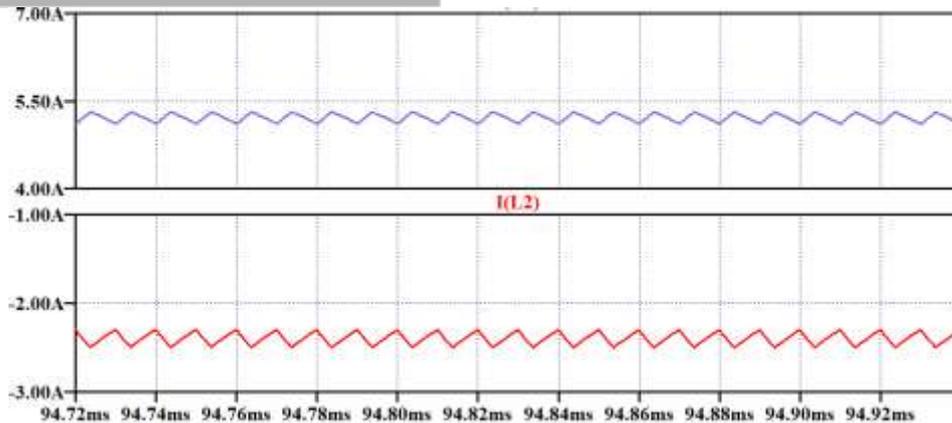
(b)

Fig 8. (a) Input voltage and current waveforms (b) Output voltage and current waveforms

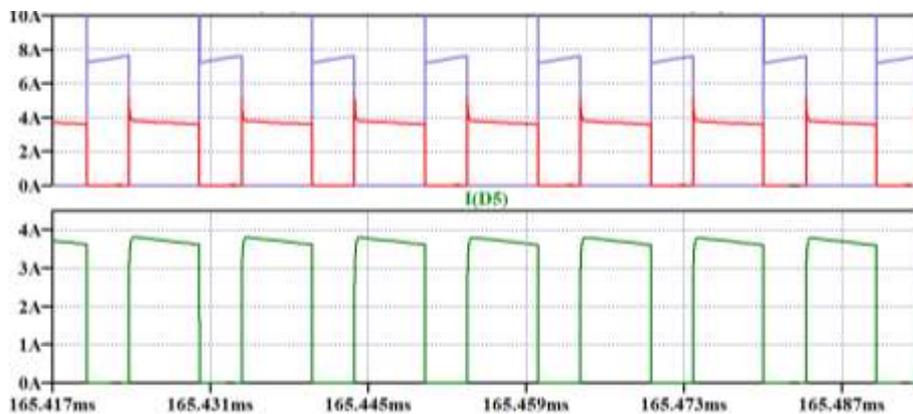


(a)

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(b)



(c)

Fig 9. (a).Capacitor voltage waveforms (b). Inductor current waveforms (c).Switch and Diode current waveforms

6. Experimental results

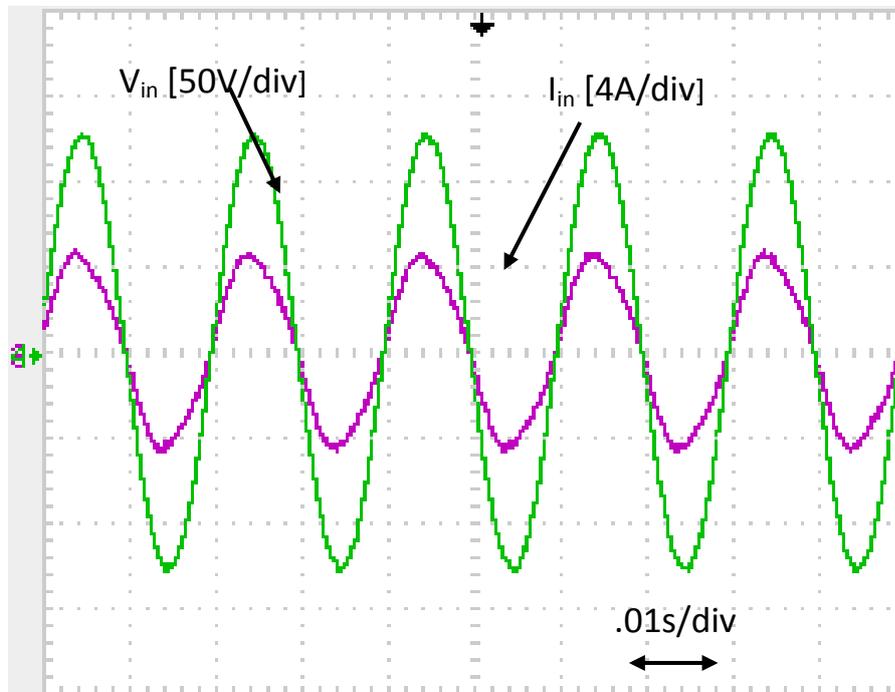
The theoretical analysis of the proposed converter is validated by experimental prototype with the same specifications of the modified bridgeless SEPIC PFC converter. Fig. 10(a) presents the experimental results of the input current and input voltage. It is noticed that the measured power factor is near to unity, since voltage and current waveforms are in phase. Output voltage and output current of the converter are shown in Fig. 10(b). Capacitor voltage and inductor current (I_{L1}) and (I_{L2}) are shown in Fig 10(c). Switch current (I_{S1}) and output diode current (I_{D0}) are presented in Fig. 10(d).From the figure it is clearly witnessed, the output diode current is nearly half to the switch current.

Fig. 11 (a) and Fig. 11 (b) illustrate input voltage, input current and output voltage, output current with change in 70% load. The output voltage of the proposed converter is regulated using compensator in the output voltage feedback loop irrespective of the load change.

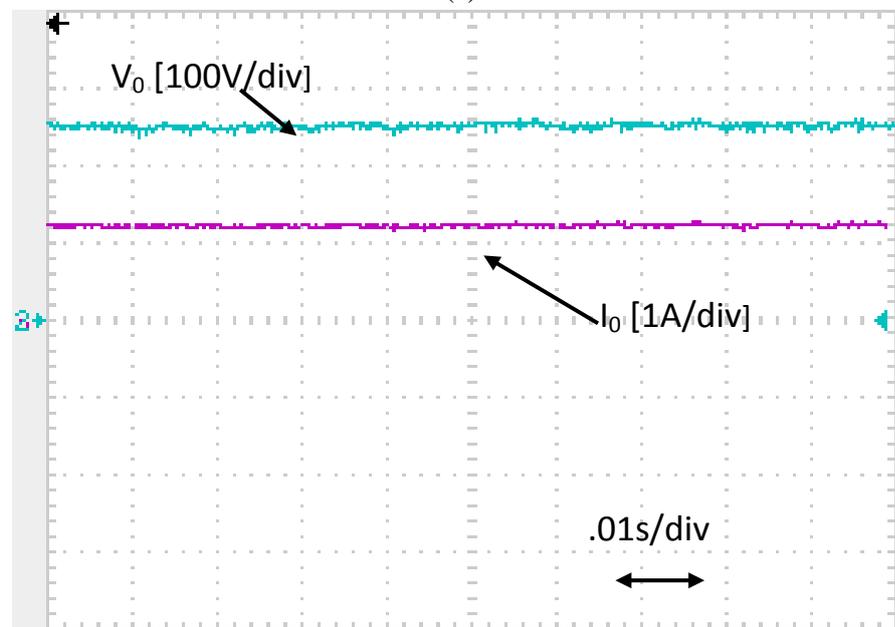
Fig. 12 (a) shows the information about experimental THD, Fig. 12 (b) presents input current harmonics in frequency domain, which is the plot between input harmonic current and harmonic order. Here input current harmonics compared with the IEC 61000-3-2 standards and also conventional CCM converter Ref.24 to show the superiority of the proposed converter. It is evident that the proposed converter input harmonic current is lower than the conventional CCM converter and

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follows the IEC 61000-3-2 standards. Fig.12 (c) shows the efficiency of the proposed converter as a function of output power in comparison with conventional and contemporary topology Ref.24. It depicts that the proposed converter shows the superior performance than the other converters at various output power.

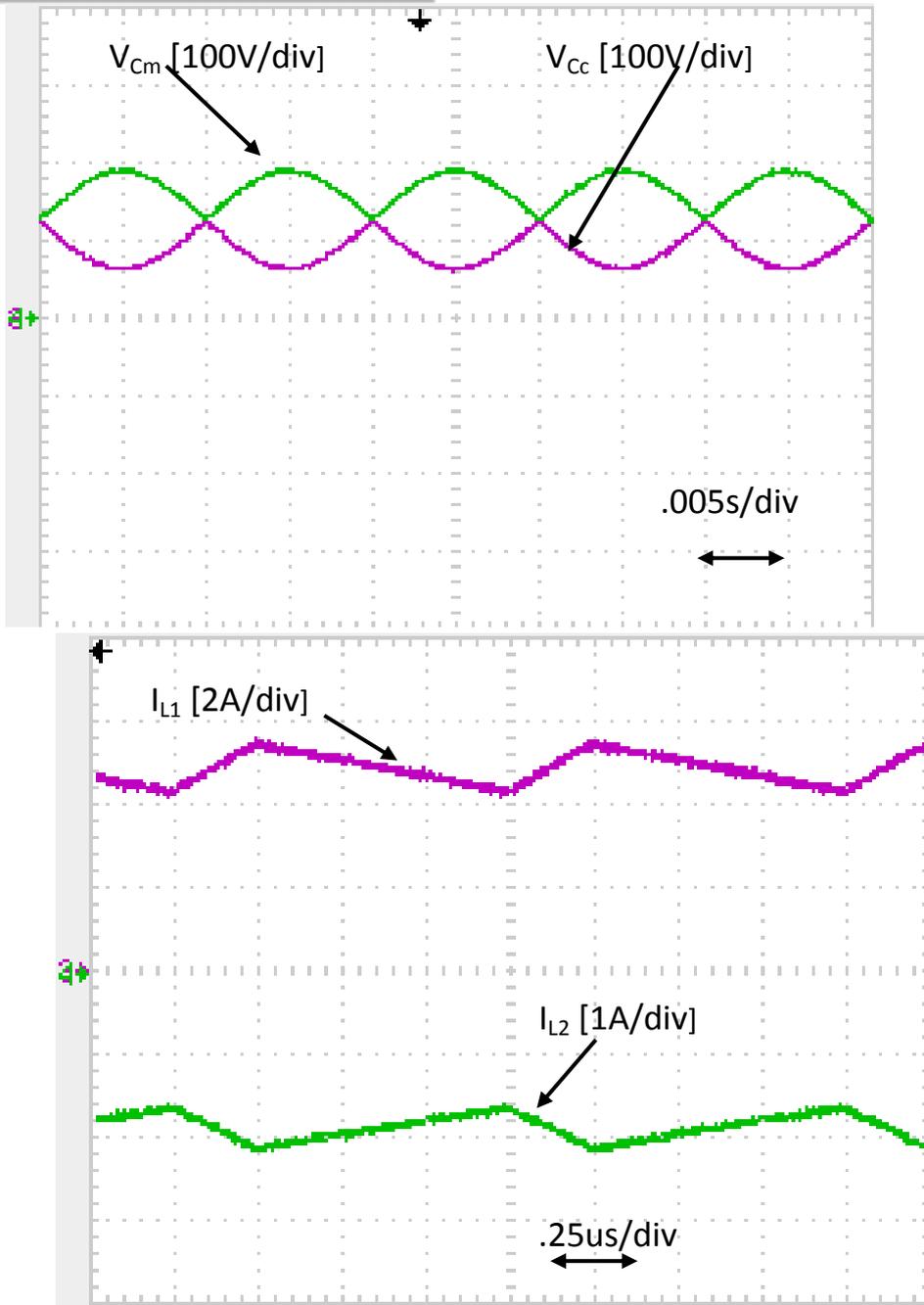


(a)

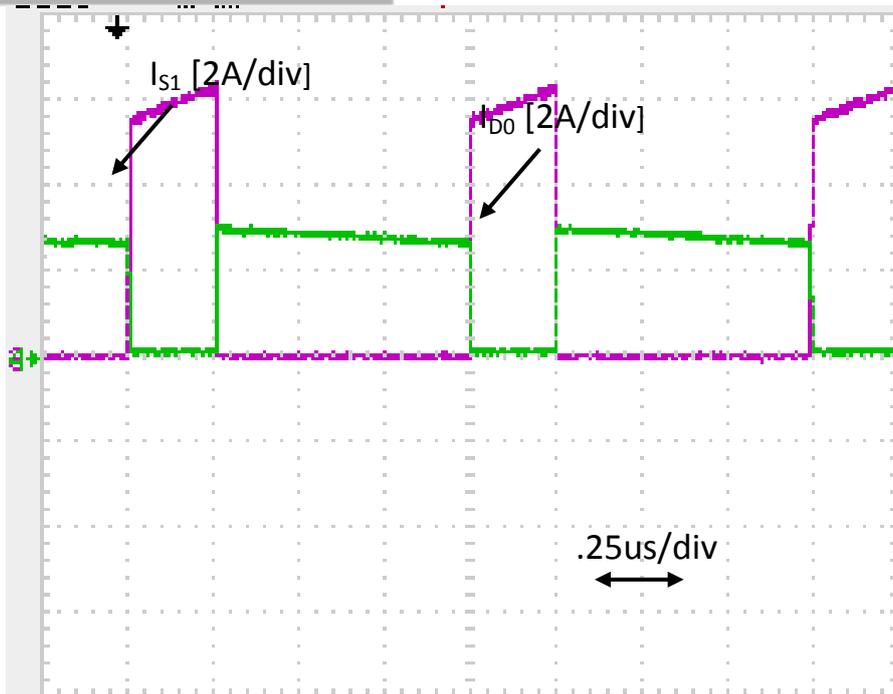


(b)

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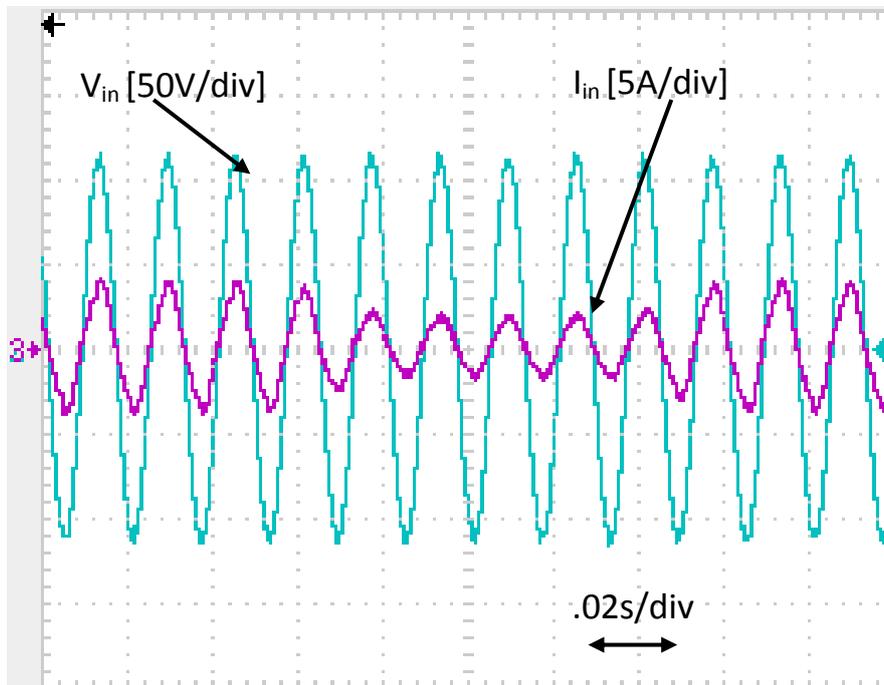


(c)

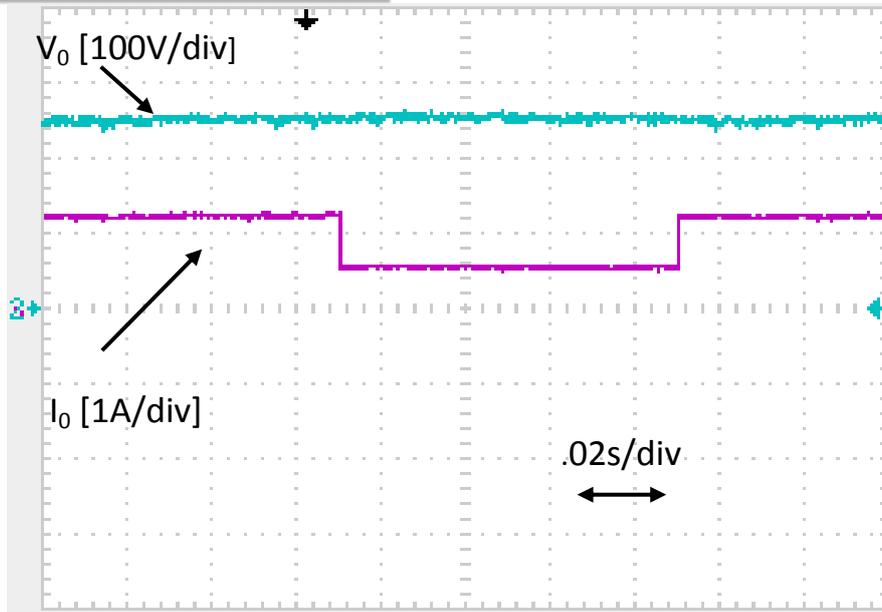


(d)

Fig 10. (a) Input Voltage and Current waveforms (b) Output voltage and Current waveforms (c) Capacitor voltage and Inductor Currents waveforms (d) Switch current and output diode current waveforms



(a)

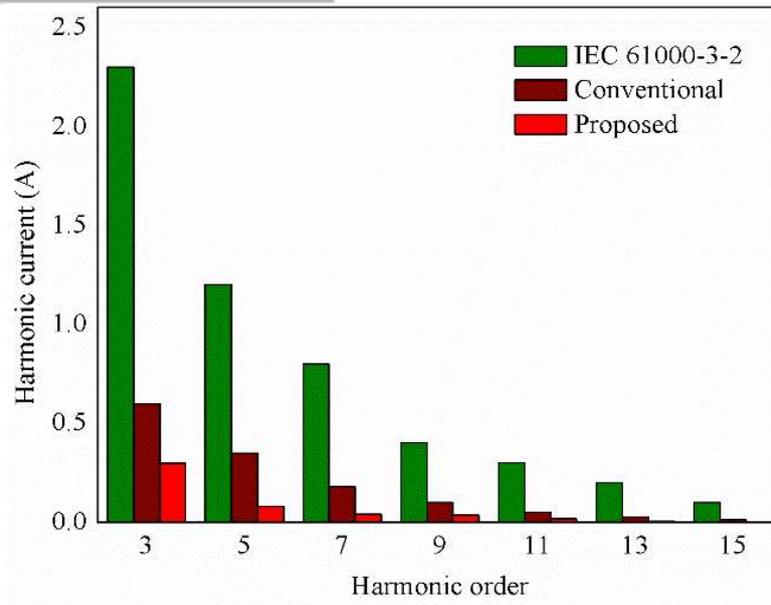


(b)

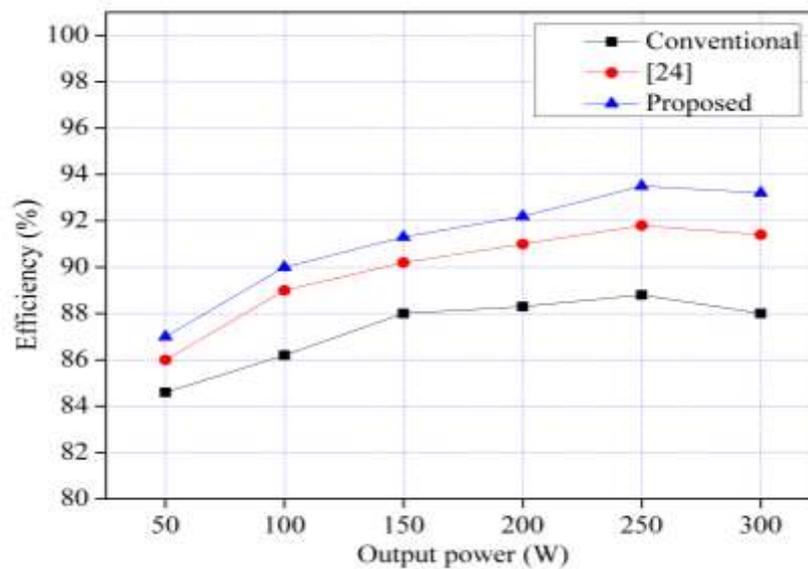
Fig 11. With load variation (a) Input voltage and current (b) Output Voltage and Output Current

PLL	U1	Or.	I1 [A]	hdf[%]	Or.	I1 [A]	hdf[%]
Freq	49.997 Hz	Tot.	3.5399		dc	-0.0087	-0.208
Urms1	85.00 V	1	3.5221	99.498	2	0.0899	2.152
Irms1	3.5399 A	3	0.3184	8.996	4	0.0629	1.507
P1	0.2949kW	5	0.1200	3.391	6	0.0010	0.025
S1	0.3000kVA	7	0.0186	0.526	8	0.0074	0.177
Q1	0.6162kvar	9	0.0112	0.319	10	0.0068	0.162
λ1	0.9855	11	0.0140	0.396	12	0.0022	0.053
φ1	69.78 °	13	0.0149	0.356	14	0.0098	0.235
		15	0.0043	0.102	16	0.0052	0.123
		17	0.0037	0.090	18	0.0010	0.023
Uthd1	1.037 %	19	0.0013	0.031	20	0.0015	0.036
Ithd1	5.298 %	21	0.0012	0.029	22	0.0021	0.050
Pthd1	0.982 %	23	0.0029	0.070	24	0.0006	0.015
		25	0.0016	0.039	26	0.0012	0.029
		27	0.0002	0.005	28	0.0010	0.024
		29	0.0004	0.009	30	0.0005	0.011
		31	0.0005	0.012	32	0.0011	0.027
		33	0.0001	0.003	34	0.0007	0.018
		35	0.0009	0.022	36	0.0002	0.005
		37	0.0002	0.005	38	0.0008	0.019
		39	0.0002	0.005	40	0.0002	0.005

(a)



(b)



(c)

Fig 12. (a) Experimental THD of source current (b) Current harmonics compared with IEC 61000-3-2 and conventional converter (c) Efficiency as a function of output power

7. Conclusion

In this study, modified bridgeless SEPIC under Continuous Conduction Mode for power factor correction is presented. The efficiency of the converter is improved and free from voltage and current stress. In addition, switch voltage is less than the output voltage and output diode current is reduced by nearly half of the switch current compared to conventional bridgeless sepic converter. It offers high static gain, lower conduction losses and suitable for high power applications. Also the switching signal applied to the switches in the circuit is same that simplifies the control. Theoretical and experimental results are provided of the proposed converter.

References

- [1]. C.M. Wang, A novel zero-voltage-switching PWM boost rectifier with high power factor and low conduction losses, *IEEE Transactions. Ind. Electron*, **52** (2005) 427–435.
- [2]. *IEC 61000-3-2*, International Electro technical Commission Genève, Switzerland, 1998
- [3]. R. Itoh et. al., Single-phase buck rectifier employing voltage reversal circuit for sinusoidal input current wave shaping, *IEE Proc. Electr. Power Appl.*, **146** (1999) 707–712.
- [4]. R. Oruganti et. al., Inductor voltage control of buck-type single-phase ac-dc converter, *IEEE Trans. Power Electron*, **15** (2000) 411–416.
- [5]. M. A. Al-Saffar et. al., Integrated buck–boost–quadratic buck PFC rectifier for universal input applications, *IEEE Trans. Power Electronics*, **24** (2009) 2886-2896.
- [6]. W. Wei et. al., A novel bridgeless buck-boost PFC converter, *IEEE power electronics specialists conference, (PESC) 2008*, pp. 1304-08.
- [7]. K. Mok et. al., A single-stage bridgeless power factor correction rectifier based on fly back topology, *IEEE international telecommunications energy conference, (INTELEC) 2011*, pp. 1-6.
- [8]. Y. Jang et. al., Bridgeless high-power-factor buck converter state-of-the-art, *IEEE Trans Ind. Electron*, **26** (2011) 602-611.
- [9]. L. Huber et. al., Performance evaluation of bridgeless PFC boost rectifiers, *IEEE Trans Power Electron*, **23** (2008)1381-1390.
- [10]. W-Y. Choi et. al., Bridgeless boost rectifier with low conduction losses and reduced diode reverse-recovery problems, *IEEE Trans Ind. Electron.*, **54** (2007) 769-80.
- [11]. E. H. Ismail, Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses, *IEEE Trans Ind. Electron*, **56** (2009)1147-57.
- [12]. K.S. Muhammad et. al., ZCS Bridgeless Boost PFC Rectifier Using Only Two Active Switches, *IEEE Trans. Ind. Electron*, **62** (2015) 2795-2806.
- [13]. A.A. Fardoun et. al., Bridgeless resonant pseudo boost PFC rectifier, *IEEE Trans. Power Electron*, **29** (2014) 5949-5960.
- [14]. A. Bouafassa et. al., Design and real time implementation of single phase boost power factor correction converter, *ISA Transactions*, **55** (2015) 267–274.
- [15]. M. Mahdavi et. al., Zero-current-transition bridgeless PFC without extra voltage and current stress, *IEEE Trans. Ind. Electron*, **56** (2009) 2540–2547.
- [16]. M. Mahdavi et. al., A new zero voltage transition bridgeless PFC with reduced conduction losses, *Jour. of Power Electron*, **9** (2009) 708–717.
- [17]. M. Mahdavi et. al., A new soft switching bridgeless PFC without any extra switch, *Int. Review. Electr. Engg*, **3** (2008) 858–863.
- [18]. A. Sabzali et. al., New bridgeless PFC Sepic and Cuk rectifiers with low conduction and switching losses, *IEEE PEDS*, pp. 873–881, 2009.
- [19]. M.R. Sahid et. al., A New AC-DC converter using bridgeless SEPIC, IEEE Annual Conf. Industrial Electronics Society (IECON 2010), pp. 286–290, November 2010.
- [20]. A. J. Sabzali et. al., New bridgeless DCM SEPIC and Cuk PFC rectifiers with low conduction and switching losses, *IEEE Trans. Ind. Appl.*, **47** (2011) 873-81.
- [21]. M. Mahdavi et. al., Bridgeless SEPIC PFC rectifier with reduced components and conduction losses, *IEEE Trans Ind. Electron*, **58** (2011) 4153-4160.

ORIGINAL ARTICLE

- [22]. Jae-won Yang et. al., Bridgeless SEPIC Converter with a Ripple –Free Input Current, *IEEE Trans. Power Electron*, **28** (2013) 3388-3394.
- [23]. C. G. Bianchin et. al., High-Power-Factor Rectifier Using the Modified SEPIC Converter Operating in Discontinuous Conduction Mode, *IEEE Transactions on Power Electronics*, **30** (2015) 4349-4364.
- [24]. J.M. Kwon et. al., Continuous-conduction-mode SEPIC converter with low reverse-recovery loss for power factor correction, *IEE Proc. Electr. Power Appl*, **153** (2006) 673-681.
- [25]. C.S. Silva, Power factor correction with the UC3854, *Unitrode Product and Applications Handbook*. (1995–96).
- [26]. L. Dixon, High. Power factor pre-regulator using the SEPIC converter, *Unitrode Product and Applications Handbook*. (1995–96).
- [27]. L.H.Dixon, Control loop design, SEPIC preregulator Example, *Unitrode Product and Applications Handbook*. (1993).