Journal of Engineering Technology
Volume 6, Issue 1, Jan. 2018, pp. 408-414

RESEARCH ARTICLE -ENGINEERNG TECHNOLOGY

A high performance grounded voltage controlled positive resistor

Charu Rana, Neelofar Afzal*, Dinesh Prasad
Jamia Millia Islamia, New Delhi, India
*Corresponding author

Abstract: A simple high performance grounded voltage controlled positive resistor (GVCPR) is proposed in this paper. The inherited features of GVCPR are simplicity, broad range of programmability, wider bandwidth and low power dissipation. The power dissipation of GVCPR measured is 22.6 μW. A programmable reciprocal circuit as an application of proposed GVCPR is also suggested. The circuits are simulated using SPICE on 0.13μm CMOS technology to demonstrate the efficacy of proposed circuits.

Keywords: CMOS, programmable, resistor, reciprocal circuit

1. Introduction

The enormous demand of portable integrated circuits for low power applications is inciting researchers to develop low power analog circuits. Low power dissipation is imperative to any battery based application for prolonged battery life [1]. One of the basic elements of analog signal processing applications is resistor. The main features considered to select a resistor for an application are accuracy, programmability and utmost low power dissipation of resistor. Several resistors have been realized [2-7] using CMOS technology and can be tuned externally. The main drawbacks of existing grounded resistors are narrow range of programmability, bandwidth, power dissipation and large silicon area. Subsequently, the blocks realized using these resistors such as modulators and oscillators [8-9] also result into undesirable high power dissipation. This paper proposes a new CMOS grounded voltage controlled positive resistor (GVCPR) which offers programmability, wider bandwidth and low power dissipation. A new programmable reciprocal circuit is also presented as an application of GVCPR.

The implementation of proposed grounded voltage controlled positive resistor (GVCPR) is given section II. Section III describes the application of GVCPR. Section IV discusses the second order effects and section V and VI show the simulation results and conclusion.

2. Proposed GVCPR

Fig. 1 shows the configuration of GVCPR comprised of seven transistors where M1, M2 and M3 are NMOS transistors and M4, M5, M6 and M7 are PMOS transistors. M1 is working in triode region whereas all other transistors are operating in saturation region. Vc is the voltage applied at gate terminal of M1 to control the resistance of the circuit for programmability. According to square law relation, the drain current equation for M1 operating in triode region is given by Eq. 1.

$$\mathrm{I1} = (\mathrm{Vc} - \mathrm{Vtn1})\mathrm{Vin} - \frac{Vin^2}{2} \quad (1)$$

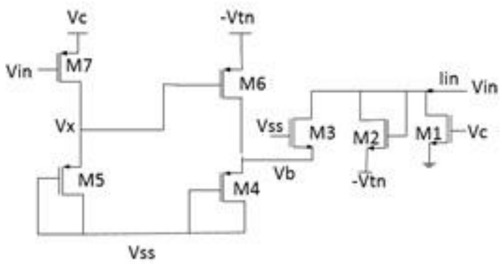

Figure. 1. Proposed GVCPR

The condition to be fulfilled for proper operation is $|Vin| = VDS1 < (VGS1 - Vtn1)$ where k1 is the transconductance parameter and Vtn1 is the threshold voltage of M1. The value of Vc should be selected greater than threshold voltage Vtn1. Transistor M2 works when Vin≥0 and its drain current can be expressed as

$$I2 = k2\left(\frac{Vin^2}{2}\right) \quad (2)$$

The gate input of M3 is generated by bias circuit consisting of transistors M4, M5, M6 and M7 operating in saturation region. It works when Vin < 0. Assuming that the transconductance parameters and threshold voltages of all transistors of bias circuit are equal then, VGS4= VGS6 and VGS5=VGS7.

$$Vc + Vin = Vx + Vss \quad (3)$$

$$Vb = Vin - Vc - Vtn \quad (4)$$

Where the value of Vss must be chosen more than Vc for desired operation.

The drain current of transistor M3 is expressed as

$$I3 = k3\left(\frac{Vin^2}{2}\right) \quad (5)$$

According to the nodal analysis, the input current Iin is summation of I1,I2 and I3 and further can be given as

$$Iin = k\big((Vc - Vtn1)Vin\big) \quad (6)$$

The transconductance parameters of M1,M2 and M3 are assumed to be same k1=k2=k3=k. The non-linear term of current I1 got cancelled by I2 and I3 for Vin≥0 and Vin<0 respectively.
Hence, the expression for input resistance is

$$Req = \frac{Vin}{Iin} = \frac{1}{k(Vc - Vtn1)} \quad (7)$$

The proposed resistor can be programmed by the voltage Vc.

3. Reciprocal Circuit

Fig. 2 shows the proposed reciprocal circuit (1/X) implemented using a PMOS based current mirror: M4 and M5 and the proposed GVCPR. It can be tuned by a bias current Iref. The gate of M1 transistor is connected to input

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voltage Vin and Vdd is equal to –Vtp. M1 is operating in linear region with gate voltage Vin more than drain voltage Vx. Iref is the summation of drain currents I1,I2 and I3 of transistors M1, M2 and M3 respectively.

Again, it is assumed that the transconductance parameters of GVCPR's transistors as well as of current mirror transistors are equal and Vout is the drain to source voltage of M1. After using Eq. (1-6) and Kirchhoff's current law, current Iref can be written as following:

$$\mathrm{Iref} = \mathrm{k}^*(\mathrm{Vin}\text{-}\mathrm{Vtn1})^*\mathrm{Vx} \quad (8)$$

$$\mathrm{Vout} = \frac{\mathrm{Iref}}{\mathrm{k}*(\mathrm{Vin}-\mathrm{Vtn1})} \quad (9)$$

Hence, reciprocal circuit is realized which can be programmed by bias current, Iref.

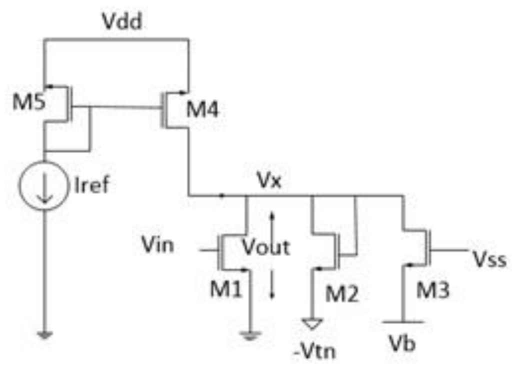

Figure. 2. Proposed Reciprocal Circuit

4. Second order effects

It is necessary to consider second order effects such as mobility degradation and mismatching of components to consider non-idealities.

4.1 Mobility Degradation

The carrier's mobility decreases under high electric field and is given by the expression:

$$\mu = \frac{\mu 0}{1-\theta(\mathrm{Vgs}-\mathrm{Vtn})} \quad (10)$$

Where μ0 is the surface mobility at room temperature, Vgs is the gate to source voltage and Vth is the threshold voltage of MOSFET. The value of mobility degradation parameter θ ranges from 0.001 V^{-1} to 0.1 V^{-1} which is extremely small and causes insignificant deviation.

4.2 Mismatching Effects

The output voltage expression of the GVCPR depends upon threshold voltage whereas reciprocal circuit output is independent of it. The mismatches in threshold voltages of transistors in GVCPR circuit can add a dc offset to expression of equivalent resistance which can be nullified by an offset applied externally. Secondly, the inequality of transconductance parameters can also cause deviation from the desired result. Assume that the k is transconductance parameter of M1 and k+ Δk of M2. The current expression given in Eq. 4 can be rewritten as follows:

Iin= I1 +I2+ΔI2 (11)

The term ΔI2 is due to Δk2 and the value of Δ k2 is much smaller to affect the expression by considerable amount. Moreover, a dc offset current can be added to circuit to nullify this mismatch.

5. Simulation Results and Comparison

The circuits proposed in this paper have been validated through simulations using SPICE in 0.13 µm CMOS technology with level 49 (Vtn = 0.0816 V, Vtp = -0.215 V, µn0 = 407.085 $cm^2/(V-s)$, µp0 = 114.645 $cm^2/(V-s)$ and Tox= 3.1 nm). The aspect ratios of all transistors of GVCPR are chosen to be 1:1. Fig. 3 shows DC characteristics of GVCPR for different values of control voltage Vc ranging from 0.6 V to 1.5 V and respective values of Req are given in the table 1. It can be seen that it is validating the analytical analysis as it functions as a linear resistor programmable by Vc with values of equivalent resistance, Req varying from 1.65 KΩ to 0.40 KΩ. It is noteworthy that the total power dissipation observed is only 22.6 µW. The frequency response of GVCPR for Req = 1.65 KΩ at Vc = 0.6 V is shown in the fig. 4 and the bandwidth obtained is 288 MHz. The total harmonic distortion (THD) measured is upto 2.7% for maximum value of Iin =50 µA. The transient analysis of GVCPR is depicted in fig. 5, sinusoidal input current of 40 µA is applied and time domain and Fourier transform response of Vin is analyzed.

The comparison of proposed GVCPR with reported literature is given in the table 2. It can be seen that the proposed GVCPR has achieved wider bandwidth and low power dissipation compared to existing resistors. The control voltage Vc ranges from 0.6 V to 2 V to tune the resistance. The supply voltages are Vdd= Vc and Vss>-Vc.

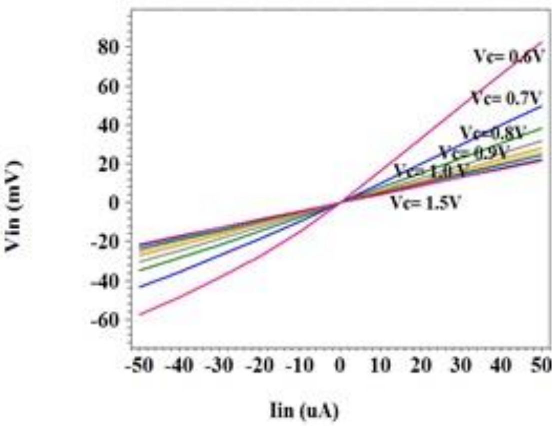

Figure 3. DC characteristics of GVCPR

The aspect ratios selected for PMOS and NMOS transistors to implement reciprocal circuit are 1:1. The DC characteristics of reciprocal circuit are shown in the fig. 6 for different value of Iref from 10 µA to 50 µA. The THD analysis with less than 2.94% is observed when input voltage from 0.5 V to 2.0 V applied separately at frequency= 1 MHz. The maximum power dissipation of reciprocal circuit achieved is 31.7 µW at Iref= 50µA which is quite remarkable. Thus, the performance of proposed reciprocal circuit is better than the existing counterpart [10].

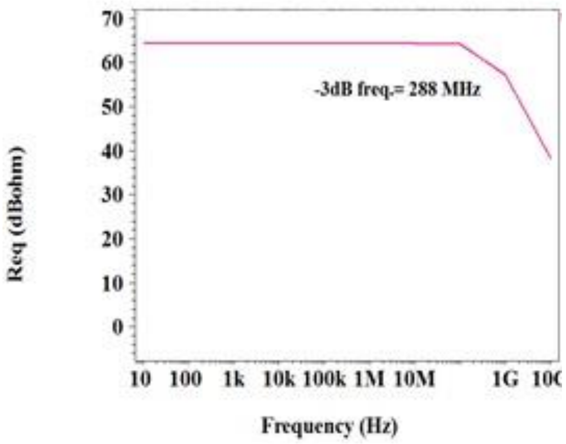

Figure 4. Frequency response of GVCPR

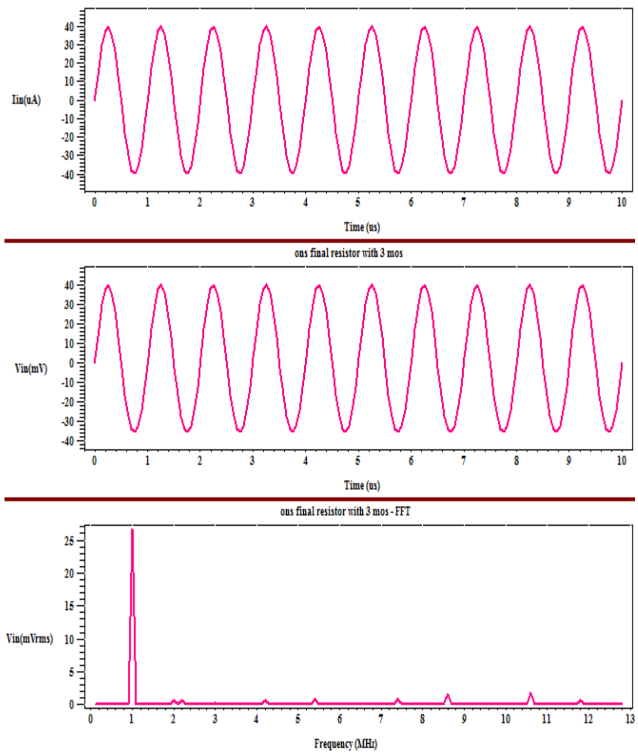

Figure 5. Transient Analysis of GVCPR

Table 1. Req values for different values of Vc

Vc(V)	0.6	0.65	0.7	1.0	1.25	1.5	2.0
Req(K Ω)	1.65	1.23	1.0	0.562	0.473	0.431	0.400

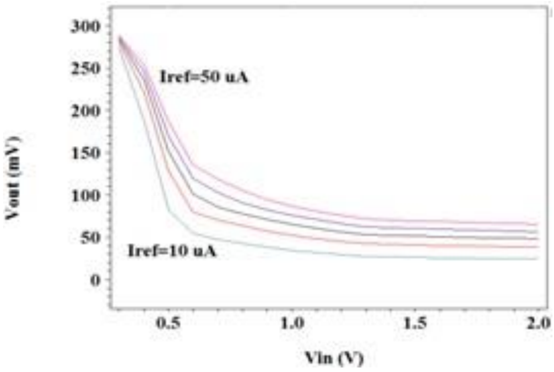

Figure 6. DC characteristics of reciprocal circuit

Table 2. Comparison of proposed GVCPR with existing resistors.

Parameters	[2]	[4]	[5]	[6]	[8]	Proposed work
No. of Transistors	9	2-MOS 3-FG MOS	1, 3- R, 1 - CCII	3	22, 2-R	7
No. of biasing voltage/currents	2	1	1	1	3	0
Technology (µm)	-	0.25	-	0.25	0.35	0.13
Supply voltages(V)	±5	±0.75	±2.5	±1.25	±1.65	Vdd=Vc Vss>-Vc
Resistance range(KΩ)	200 to 60	4 to 2	-	<2.63	15 to 5	1.65 to 0.40
Power dissipation (µW)	-	254	-	440	2600	22.6
Bandwidth (MHz)	-	-	-	>100	100	288
Control Voltage Range(V)	2.4 to 3.3	0.10 to 0.75	-	0.65 to 2.0	00,10, 01	0.60 o 2.0

6. Conclusion

This paper proposes a new grounded voltage controlled positive resistor with power dissipation of only 22.6 μW and bandwidth of 288 MHz. GVCPR can be programmed while validating the claimed theoretical results by simulation results. Programmable reciprocal circuit is also presented as an application of GVCPR. These blocks are believed to be beneficial for high performance analog applications.

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