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A novel mitigation algorithm for switch open-fault in parallel inverter topology fed induction motor drive

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Abstract: Faults in circuits with power electronic static switches are wide spread to arise and more common in converters like inverters. Inverters are circuits which converters from DC type of supply to AC with help of power electronic static switches. Diode clamped inverters are subjected to faults and mitigation of fault is at prior important to restore normal operation of connected load. This paper introduces the novel fault mitigation algorithm for switch open type of fault in parallel inverter topology fed induction motor load to increase the reliability. The proposed methodology recognizes the integration of two parallel diode clamped inverters for sharing to drive the induction motor load which reduces the rating of devices and losses. Diode clamped inverters are controlled using asymmetrical PWM technique. Proposed work was carried out using MATLAB/SIMULINK software and simulation results were presented showing inverter performance and induction motor performance characteristics.

Keywords: Fault Mitigation Algorithm, Induction Motor Drive, Open Fault, Three-Phase Parallel Inverter Topology.

1. Introduction

Fault in power electronic devices is inadvertent open or short circuit of power switching cells in system. Faults in power electronic systems are very common in occurrence and might occur due o system unusual behavior. Types of faults in power electronic circuits include diode open fault, diode short fault, gate open, gate short fault, power switch (IGBT) open and short faults out of which switch open and short faults are considered the most to occur and constitutes around 40% of the total faults [1]-[3]. Open type of fault in inverter is refereed in this paper in general and need to consider as open fault wherever fault is mentioned. Thermal issues like over voltage or over-current might be a possible reason for fault occurrence in power electronic circuit. Mechanical issues and insulation breakdown may be also the reason for fault production in power converters. Improper manufacturing, polluted insulation, switching surges and improper installations are also reasons for faults [4]-[7]. The main motivation is a new challenge for power engineers to protect power electronic converters which are now-a-days used in almost every circuit systems against these faults to ensure reliability and continuity in supply to the connected loads.

Induction motor dives are most used drives in industries due to its constructional advantages like simple and robust with less maintenance required. Induction motors fed from inverters showcase many advantages over conventional methods of speed control of induction motor as terminal voltage and frequency both can be controlled at the same time with inverter thus rotating motor at required and rated speeds as desired [8]. A single diode clamped inverter fed induction motor shown in Fig.1, is responsible of handling the total load rating and if any fault condition in inverter can affect the

overall system performance of the system and load. Even the reliability and providing continuity of supply to the system can be a question in that condition. The importance of study is proposing a new parallel inverter topology, it can address the issue of continuous power supply and increasing the reliability of supply. Even the rating of switching components in parallel inverters is reduced due to load sharing and overall switching losses get reduced [9]. Fault condition in inverter fed induction motor is to be mitigated to ensure power outage in the system. Fault condition in one out of two parallel inverters sharing load of induction motor is main benefit, it overcomes the malfunction of load degrading its performance affecting load characteristics. This paper presents the simple algorithm for fault identification in phase of parallel inverter topology fed induction motor drive and to mitigate open fault. Two parallel inverter topology share the load of induction motor was carried out using MATLAB/SIMULINK software and results were presented considering different conditions. Fault analysis and mitigation was presented if fault exists only in upper and only in lower inverters of two parallel inverter topology and analysis for mitigation was also presented with fault in both the parallel inverters.

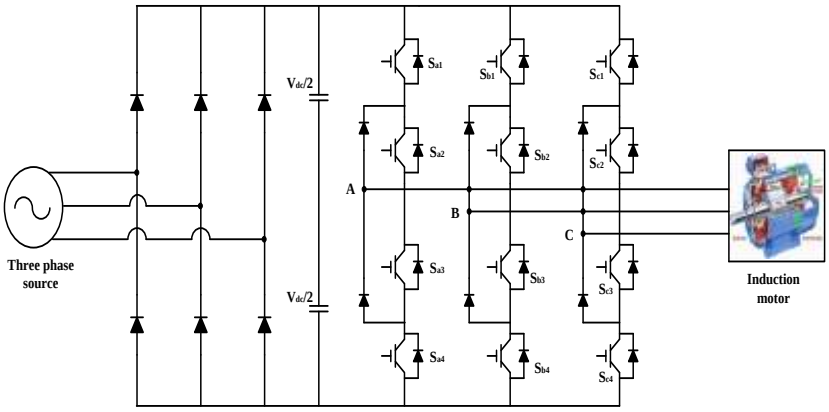

Fig.1 Conventional Diode Clamped Inverter Fed Induction Motor

2 Two Parallel Inverter Topology for Induction Motor Drive

Two parallel inverters topology for induction motor drive is developed to share the load such that the rating of power devices in individual inverters gets reduced and as a result conduction losses reduce. Fig. 2 shows the two parallel inverter topology for induction motor. The source AC type is fed to individual inverters through diode bridge rectifiers. Diode bridge rectifiers' converters AC type of supply to DC and feeds diode clamped inverter in each parallel path. The converted DC is fed to AC through diode bride inverter in each bridge. The combined output from two parallel inverters feed induction motor load. Diode clamped inverters consists of power switches and diodes. Diodes are used as clamping elements in multi-level diode clamped inverter topology.

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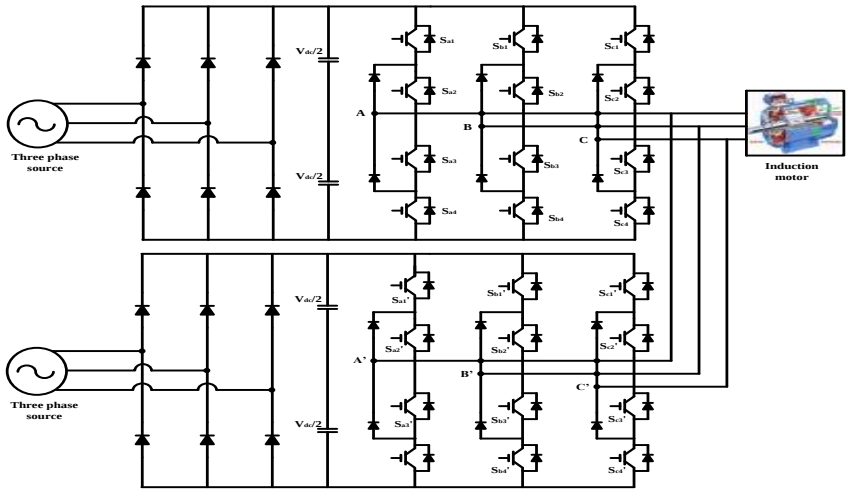

Fig.2 Two Parallel Inverter Topology Fed Induction Motor

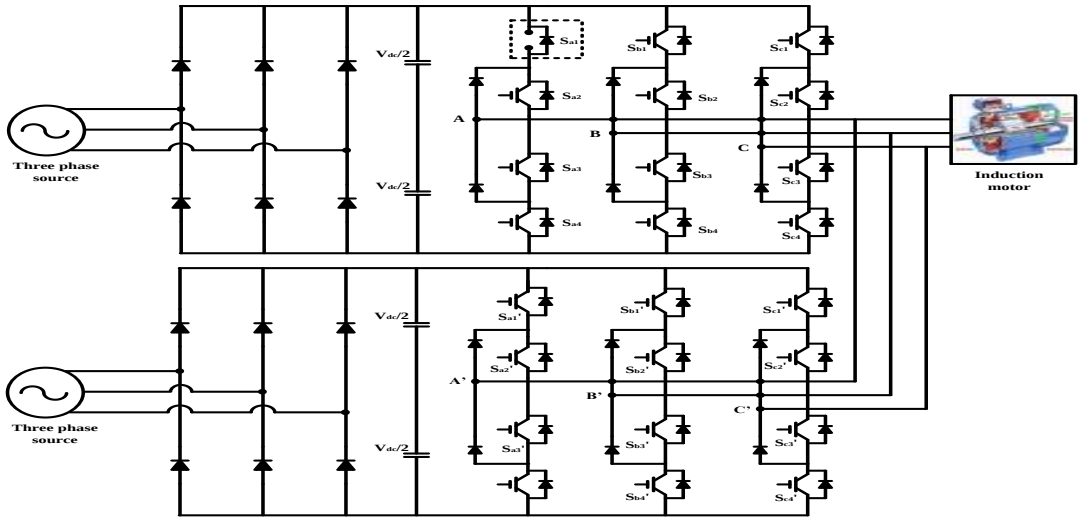

Fig.3 Fault in Upper Inverter of Two Parallel Diode Clamped Inverter Topology

3 Fault Analysis in Diode-Clamped Inverter Topology

Two-parallel inverter topology feeding an induction motor load with open type of fault in only upper inverter of two was shown in Fig.3. Fault existing in only lower inverter of two- parallel inverter topology when the other inverter (upper inverter) stays healthy was shown in Fig.4. Fault in both the parallel inverters is depicted in Fig.5. Diode clamped inverters consists of power electronic static switches and faults like power switch open and short circuit. Switch open type of fault is illustrated in proposed work. Switch open fault can deviate the inverter output line voltages and phase voltages along with line currents. Deviation in line currents and inverter voltages can disturb the normal operation of induction motor drive connected as load and induction motor drive malfunctions. Parallel inverter concept was introduced to share the load of induction motor such that the individual switching ratings will be reduced. Switch ratings reduction can eventually lead to reduced losses in inverter circuit. Fault identification is as much important to mitigate the fault condition in inverter.

Fault mitigation increases the tolerance of the machine drive. Fault identification in inverter is the initiation to fault mitigation and prior knowledge of fault in inverter circuit can increase the rate of fault identification. Parallel inverter topology increases the reliability of system.

4 Proposed Fault Mitigation Analysis in Diode-Clamped Inverter Topology

Fault mitigation is very important phenomenon to restore the basic function of circuit. Fault mitigation algorithm to identify and mitigate the open fault condition in two-parallel diode clamped inverter is shown in figure 6. Initially line currents in three phases of inverter are measured. The measured currents are recorded for harmonic distortion and if found the distortion greater than 10% in a particular phase concludes the existence of fault in that particular phase of inverter. If harmonic distortion in line current in any particular phase is less than 10% indicates that there is no fault condition. The identified fault in any phase of inverter is mitigated with modulated waves of other two healthy phases of inverter maintaining 120^0 phase shift between them. The faulty phase amplitude along with phase is made zero while the other two phases are fed with phases -150^0 and 30^0 such that the effective phase shift between two healthy phases is 120^0 maintained with asymmetrical PWM technique. The faulty phase is isolated and induction motor is driven with only two active phases producing rotating magnetic flux and runs with normal operation. The frequency is kept constant with fundamental component in all healthy phases with unit amplitude. Two-parallel inverter topology fed induction motor drive with fault mitigation algorithm is shown in Fig. 7.

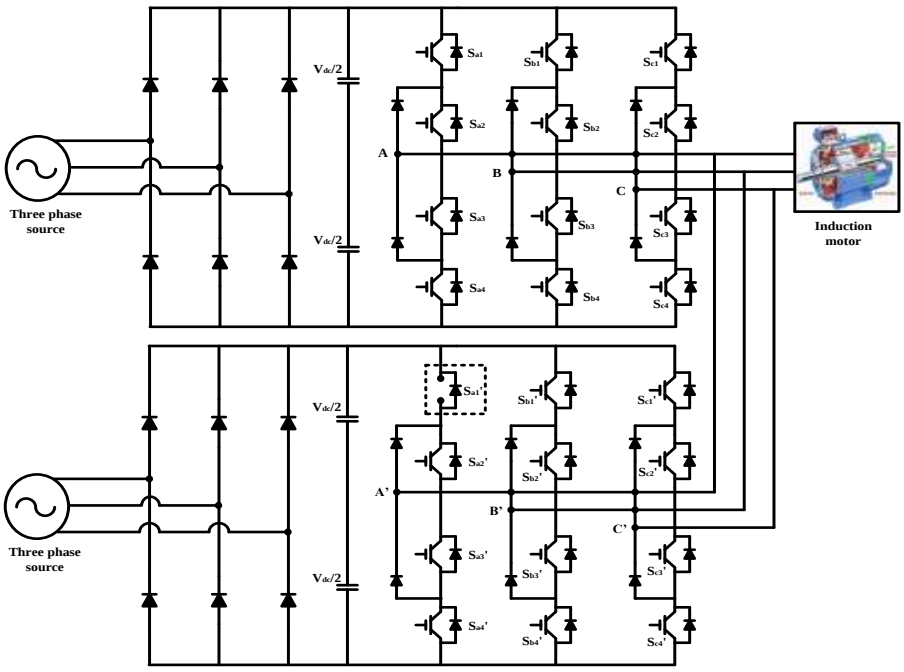

Fig.4 Fault in lower inverter of two parallel diode clamped inverter topology

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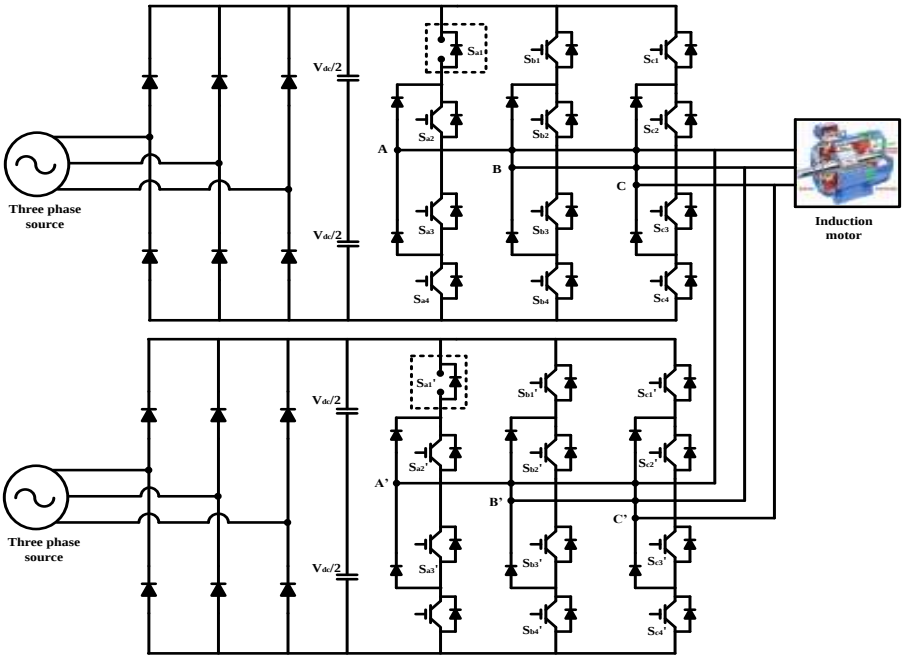

Fig.5 Fault in both parallel diode clamped inverters

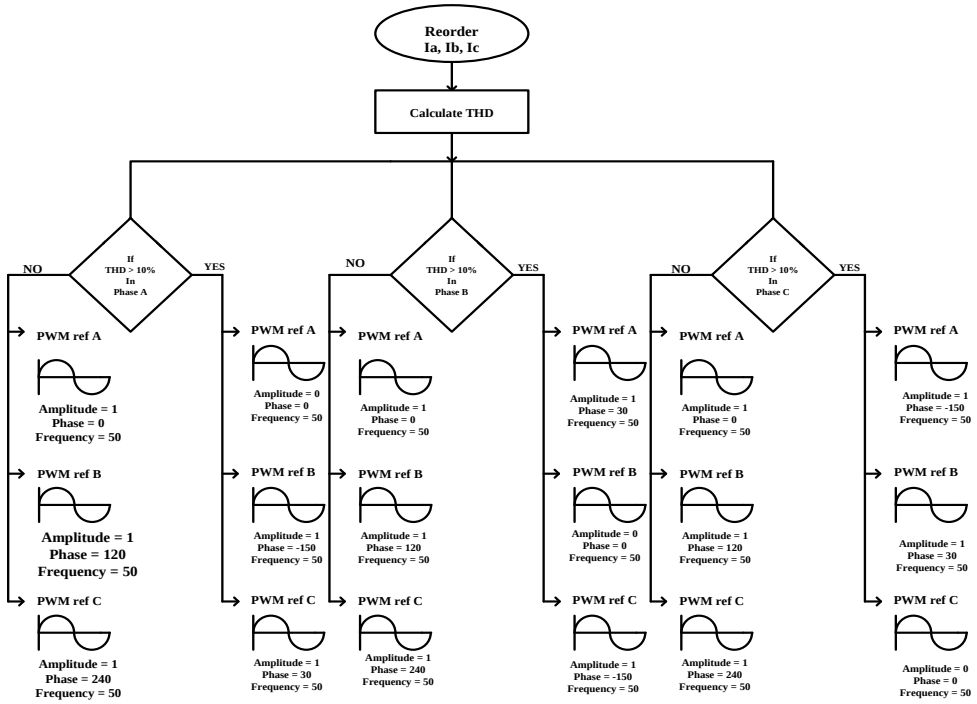

Fig.6 Fault Mitigation Algorithm

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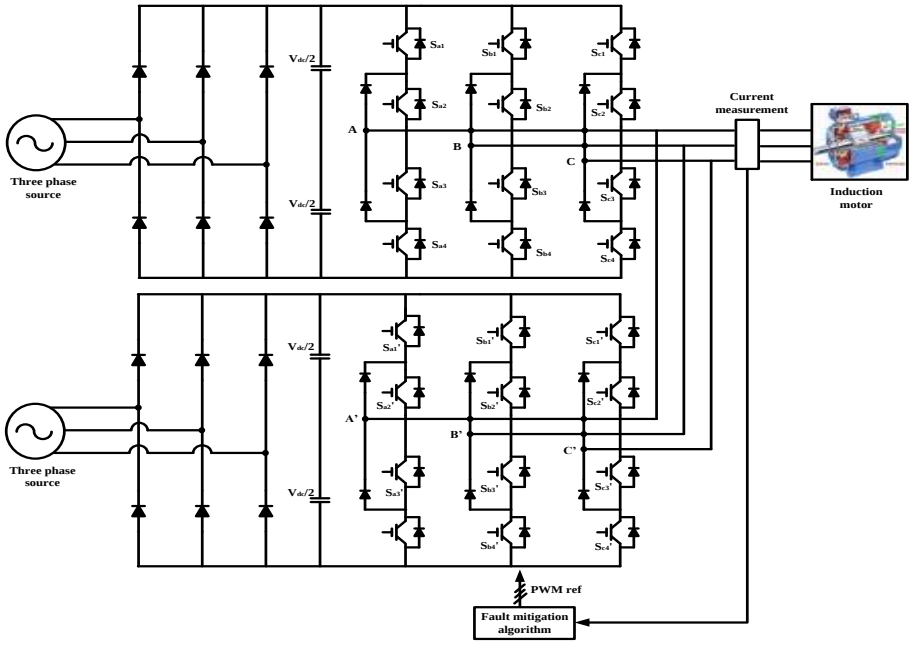
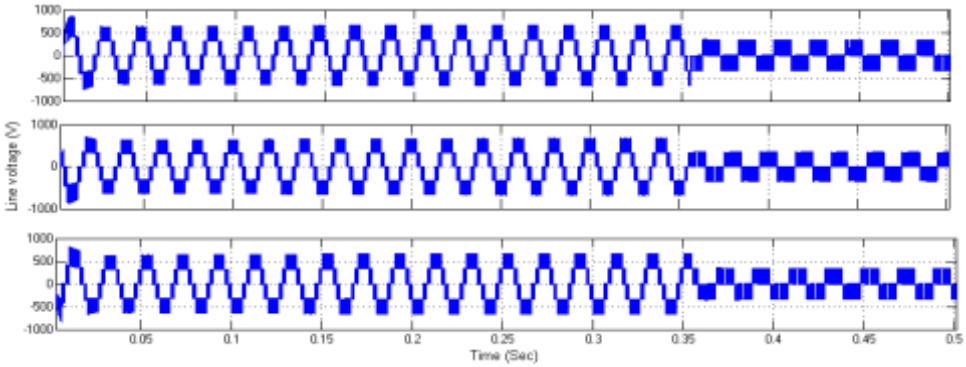


Fig.7 Parallel Diode Clamped Inverter with Fault Mitigation Algorithm

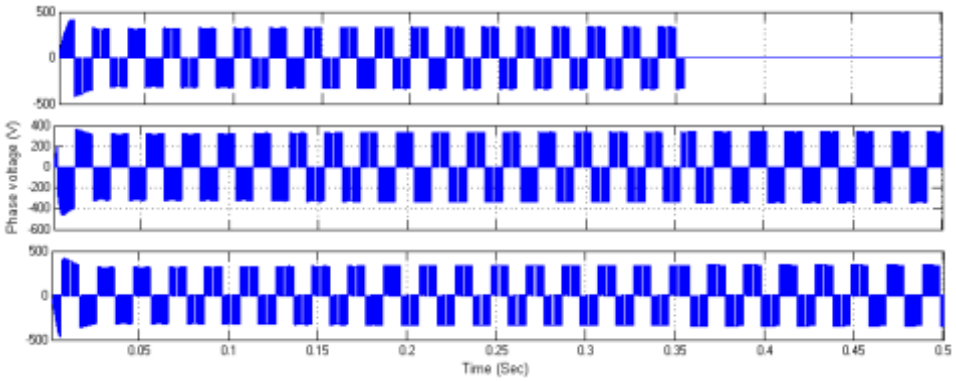
5 Simulation Results and Discussion

Analysis for fault mitigation was carried out with fault in only one of the either inverters in two-parallel inverter topology and with fault in both inverters. Fault was introduced at 0.35 seconds and mitigation was shown for all cases.

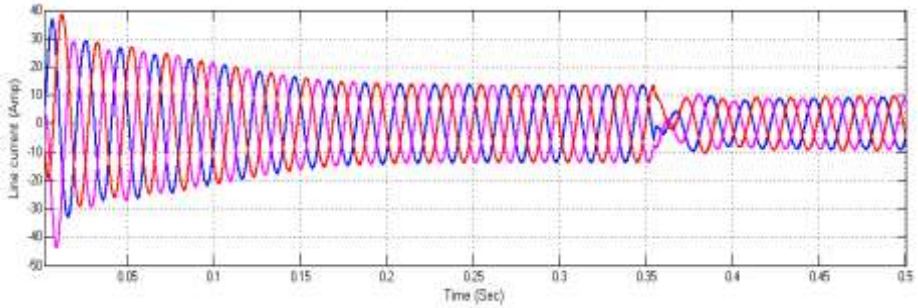
5.1 Fault in Only Phase-A of Upper Inverter



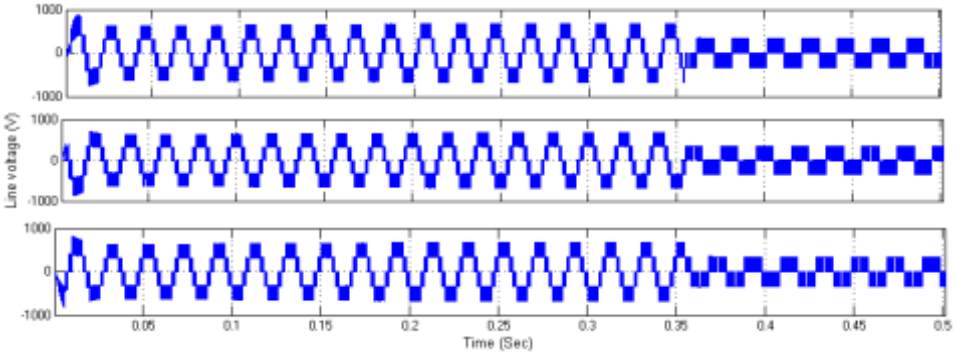
(a) Line voltage of upper inverter



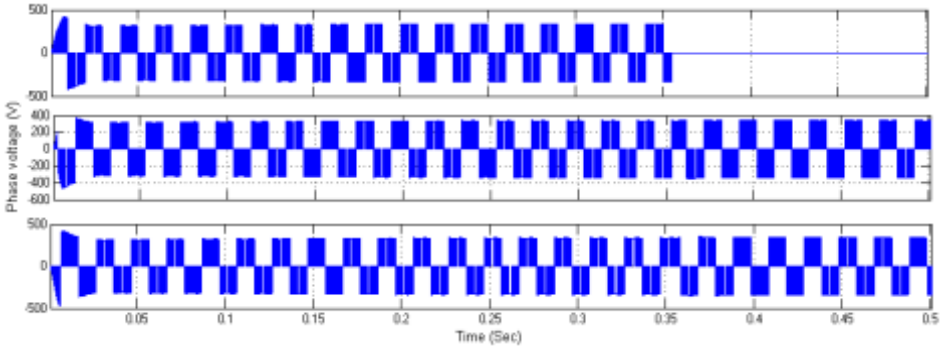
(b) Phase voltage of upper inverter



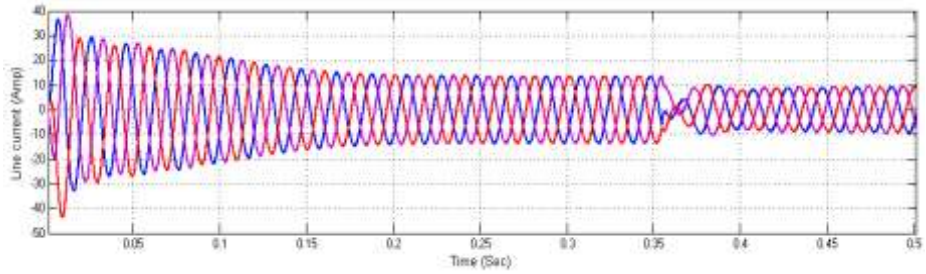
(c) Line currents of upper inverter



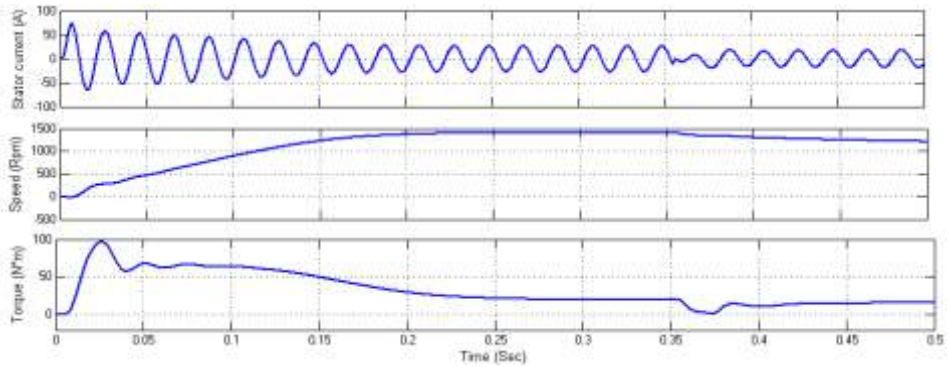
(d) Line voltage of lower inverter



(e) Phase voltage of lower inverter



(f) Line currents of lower inverter



(g) Induction motor characteristics

Fig.8 Simulation Outcomes of Fault in Phase-A of Upper Inverter Only

Fig.8 shows the simulation outcomes of open fault in phase-A of upper inverter only, in that (a) Line voltage of upper inverter, (b) Phase voltage of upper inverter, (c) Line currents of upper inverter, (d) Line voltage of lower inverter, (e) Phase voltage of lower inverter, (f) Line currents of lower inverter, (g) Induction motor characteristics. At normal instant, phase voltages & line voltages of upper inverter under fault in phase-A of upper inverter is normal in shape with no distortion, at faulty instant the line voltages tends to distort but due to fault mitigation the line voltages remains with normal shape in phases of inverter with reduced magnitude indication no power outage fed to induction motor. At faulty instant the line voltages tends to distort but due to fault mitigation the line voltages remains with normal shape in phase-B and phase-C while phase-A is discontinued from circuit with asymmetrical PWM signal not triggering Phase-A of inverter. The Line current of upper inverter is observed to be 15A sharing half of the total load current of 30A. The line current is slightly distorted at fault instant and resumed normal shape after fault mitigation. At normal instant, phase voltages & line voltages of lower inverter are normal in shape with no distortion, at faulty instant the line voltages tends to distort but due to fault mitigation the line voltages of lower inverter remains with normal shape in phases of inverter with reduced magnitude indication no power outage fed to induction motor. At faulty instant the line voltages of lower inverter tends to distort but due to fault mitigation the line voltages remains with normal shape in phase-B and phase-C while phase-A is discontinued from circuit with asymmetrical PWM signal not triggering Phase-A of inverter. The Line currents of lower inverter are observed to be 15A sharing half of the total load current of 30A and the line current is slightly distorted at fault instant and resumed normal shape after mitigation. An induction motor characteristic with open fault in upper inverter represents the stator current, speed and torque curves. Before fault instant, stator current is with 30A peak constant and speed maintained at 1500 RPM with torque at 20 Nm. After fault mitigation the characteristics regains normal values indicates no outage in induction motor supply with fault in one phase of inverter.

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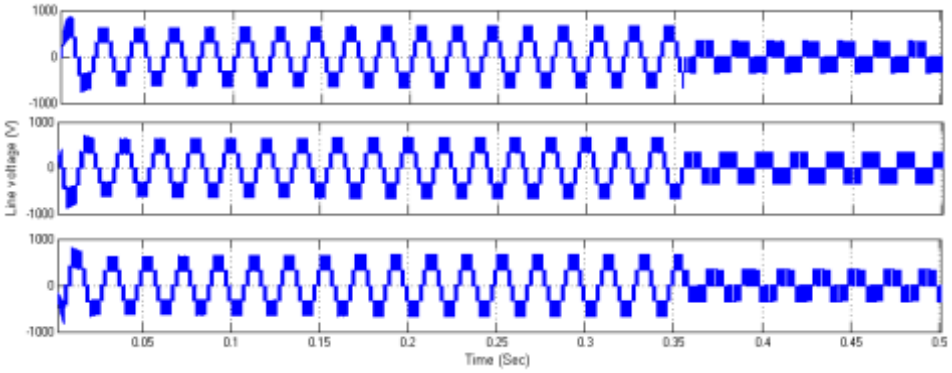
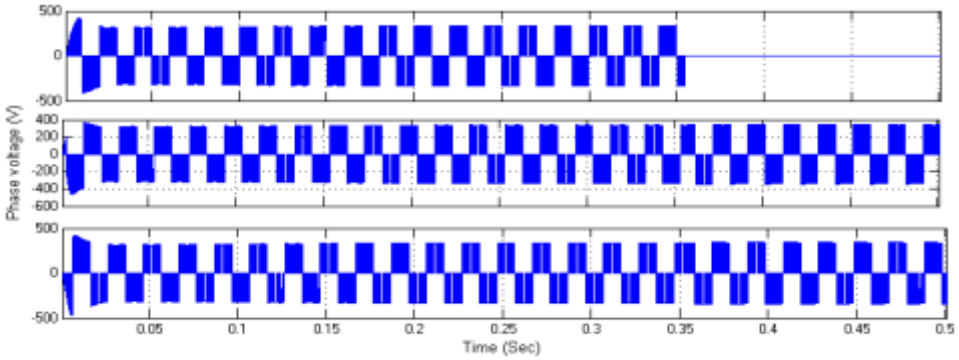
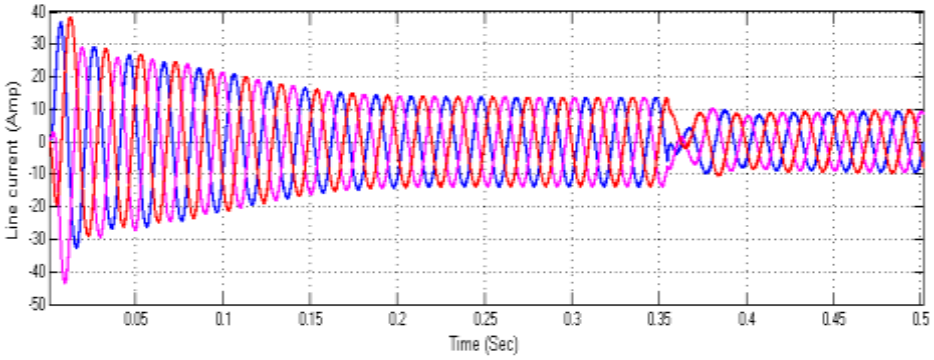
5.2 Fault in Only Phase-A of Lower Inverter



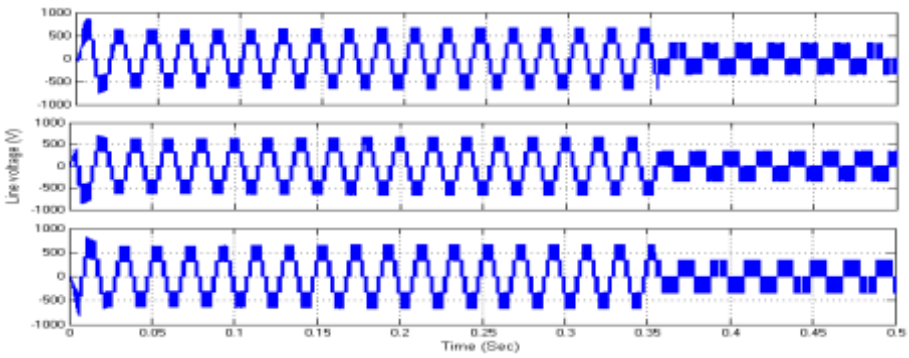
(a) Line voltage of upper inverter



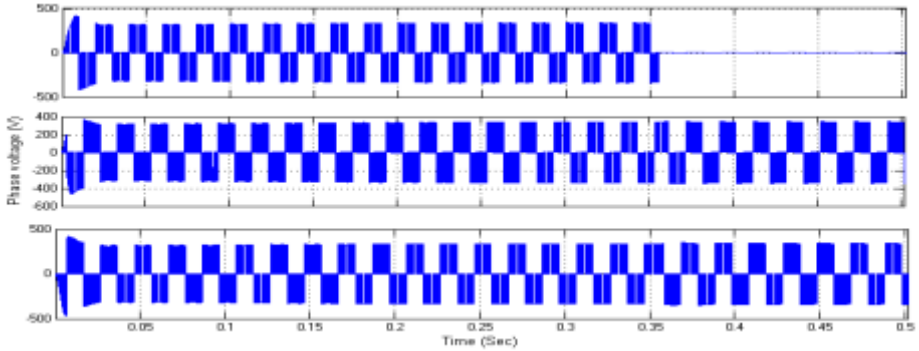
(b) Phase voltage of upper inverter



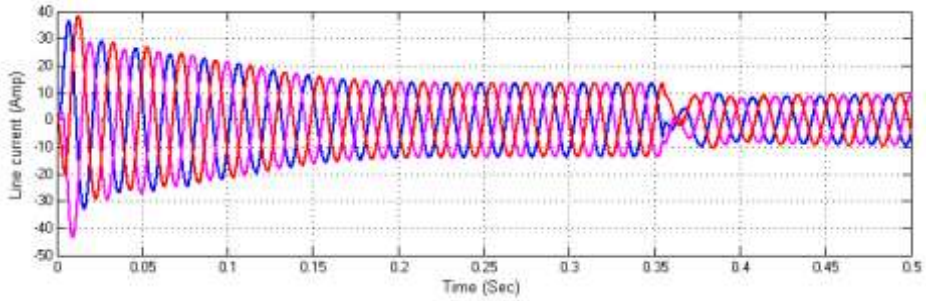
(c) Line currents of upper inverter



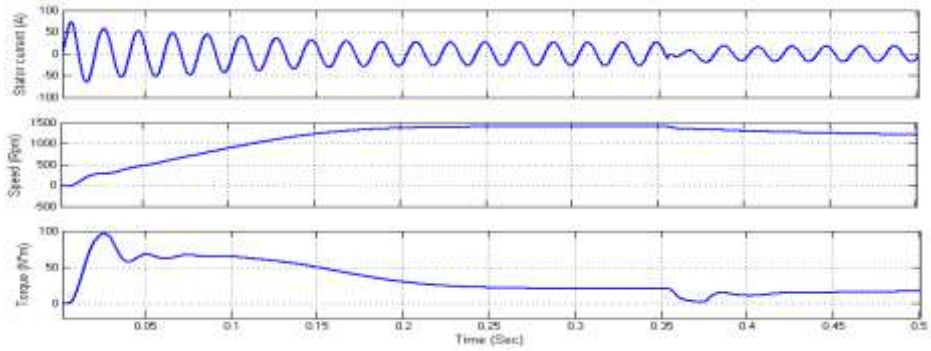
(d) Line voltage of lower inverter



(e) Phase voltage of lower inverter



(f) Line currents of lower inverter



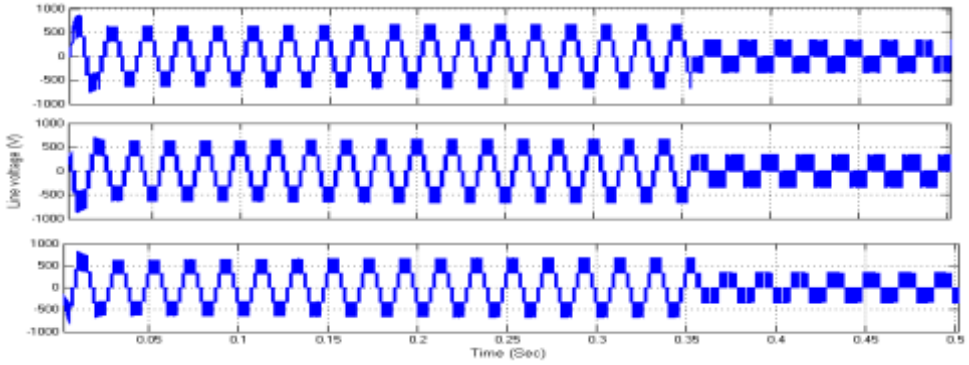
(g) Induction motor characteristics

Fig.9 Simulation Outcomes of Fault in Phase-A of Lower Inverter Only

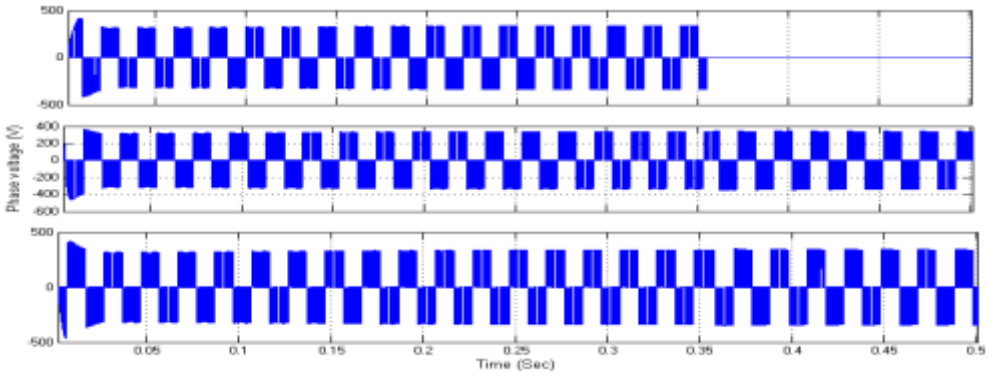
Fig.9 shows the simulation outcomes of open fault in phase-A of lower inverter only, in that (a) Line voltage of upper inverter, (b) Phase voltage of upper inverter, (c) Line currents of upper inverter, (d) Line voltage of lower inverter, (e) Phase voltage of lower inverter, (f) Line currents of lower inverter, (g) Induction motor characteristics. At normal instant, phase voltages & line voltages of upper inverter under fault in phase-A of lower inverter is normal in shape with no distortion, at faulty instant the line voltages tends to distort but due to fault mitigation the line voltages remains with normal shape in phases of inverter with reduced magnitude indication no power outage fed to induction motor. At fault instant the line voltages of upper inverter tends to distort but due to fault mitigation the line voltages remains with normal shape in phase-B and phase-C while phase-A is discontinued from circuit with asymmetrical PWM signal not triggering Phase-A of inverter. The Line current of upper inverter is observed to be 15A sharing half of the total load current of 30A. The line current is slightly distorted at fault instant and resumed normal shape after mitigation. At normal instant, phase voltages & line voltages of lower inverter under fault in phase-A of lower inverter is normal in shape with no distortion, at fault instant the line voltages tends to distort but due to fault

mitigation the line voltages remains with normal shape in phases of inverter with reduced magnitude indication no power outage fed to induction motor. At fault instant the line voltages of lower inverter tends to distort but due to fault mitigation the line voltages remains with normal shape in phase-B and phase-C while phase-A is discontinued from circuit with asymmetrical PWM signal not triggering Phase-A of inverter. The line current is observed to be 15A sharing half of the total load current of 30A. The line current is slightly distorted at fault instant and resumed normal shape after mitigation. An induction motor characteristic with open fault in lower inverter represents the stator current, speed and torque curves. Before fault instant, stator current is with 30A peak constant and speed maintained at 1500 RPM with torque at 20 Nm. After fault mitigation the characteristics regains normal values indication no outage in induction motor supply with fault in one phase of inverter.

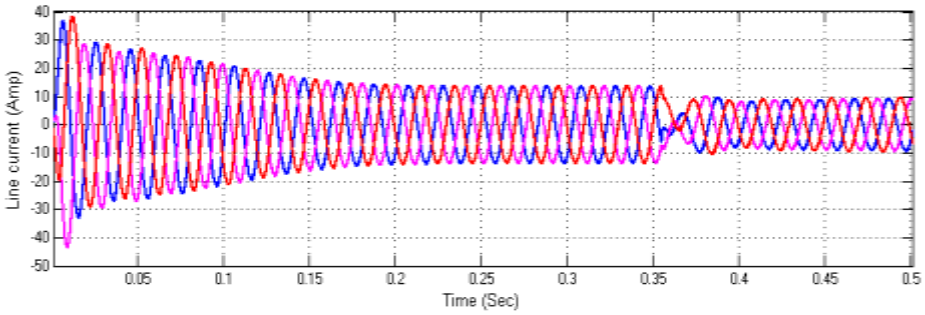
5.3 Fault in Only Phase-A of Both Upper & Lower Inverters



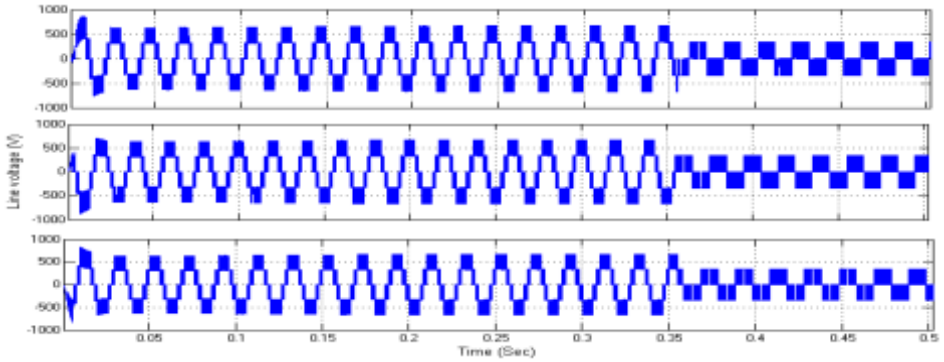
(a) Line voltage of upper inverter



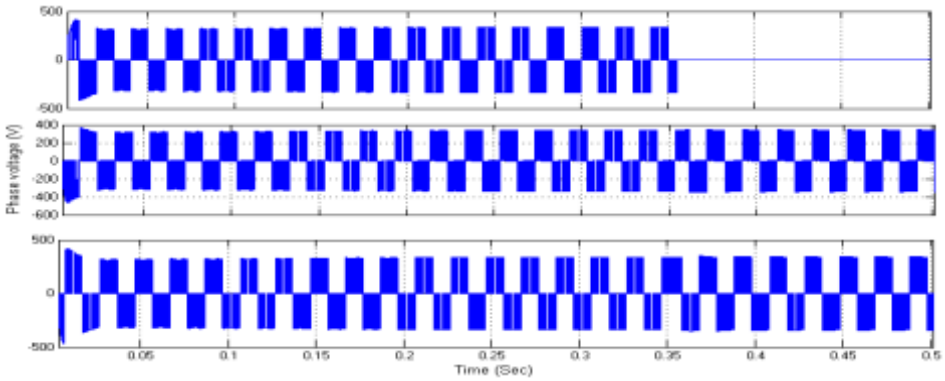
(b) Phase voltage of upper inverter



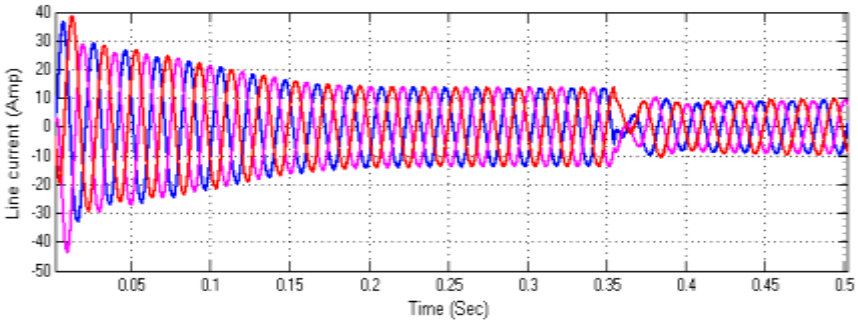
(c) Line currents of upper inverter



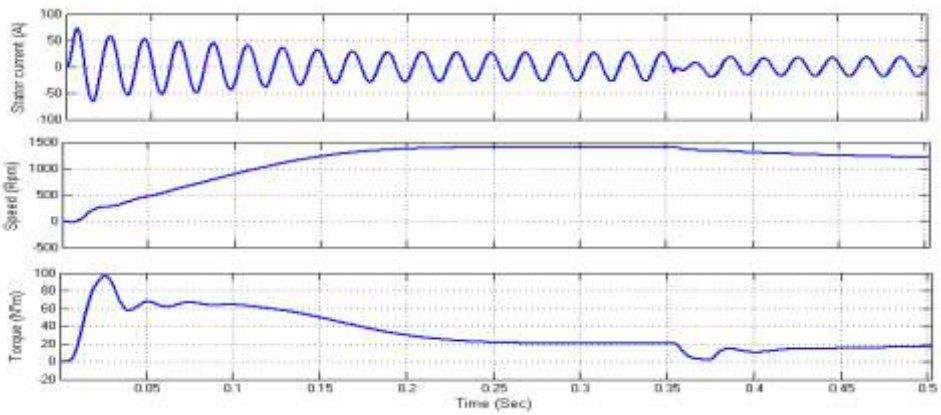
(d) Line voltage of lower inverter



(e) Phase voltage of lower inverter



(f) Line currents of lower inverter



(g) Induction motor characteristics

Fig.10 Simulation Outcomes of Fault in Phase-A of both Upper & Lower Inverters

Fig.10 shows the simulation outcomes of open fault in phase-A of both upper & lower inverters, in that (a) Line voltage of upper inverter, (b) Phase voltage of upper inverter, (c) Line currents of upper inverter, (d) Line voltage of lower inverter, (e) Phase voltage of lower inverter, (f) Line currents of lower inverter, (g) Induction motor characteristics. At normal instant, the phase & line voltages under the phase-A open-fault of both inverters is normal in shape with no distortion, at faulty instant the line voltages of upper inverter tends to distort but due to fault mitigation the line voltages remains with normal shape in phases of inverter with reduced magnitude indication no power outage fed to induction motor. At faulty instant the line voltages of upper inverter tends to distort but due to fault mitigation the line voltages remains with normal shape in phase-B and phase-C while phase-A is discontinued from circuit with asymmetrical PWM signal not triggering Phase-A of inverter. The line current of upper inverter is observed to be 15A sharing half of the total load current of 30A. The line current is slightly distorted at fault instant and resumed normal shape after mitigation. The Line 7 phase voltage of lower inverter with fault in phase-A of both parallel inverters represents the line voltage & phase voltages. At normal instant, phase & line voltages of lower inverter are normal in shape with no distortion, at fault instant the line voltages tends to distort but due to fault mitigation the line voltages remains with normal shape in phases of inverter with reduced magnitude indication no power outage fed to induction motor. At fault instant the line voltages of lower inverter tends to distort but due to fault mitigation the line voltages remains with normal shape in phase-B and phase-C while phase-A is discontinued from circuit with asymmetrical PWM signal not triggering Phase-A of inverter. The line current of lower inverter is observed to be 15A sharing half of the total load current of 30A. The line current is slightly distorted at fault instant and resumed normal shape after mitigation. An induction motor characteristic with open fault in both upper and lower inverters represents the stator current, speed and torque curves. Before fault instant, stator current is with 30A peak constant and speed maintained at 1500 RPM with torque at 20 Nm. After fault mitigation the characteristics regains normal values indication no outage in induction motor supply with fault in phase of inverters.

6 Conclusion

The paper presents an algorithm for fault mitigation in two-inverter topology of diode clamped inverter fed induction motor drive. The proposed algorithm is capable of mitigating the open type of fault in switching cell and was validated in different conditions like introducing fault in only one inverter of two-inverter topology and also by introducing fault in both the parallel inverters. Line currents shown indicate the load sharing among the parallel inverters and induction motor characteristics shows the validation of algorithm to mitigate the fault effectively. The further recommendation carried on higher voltage levels by introducing novel MLI topologies.

References

[1] Baran, M.E. and El-Markaby, I. "Fault Analysis on Distribution Feeders with DG." IEEE Transaction, 2005

[2] BDEW. Technical Guideline "Generating Plants Connected to Medium-Voltage Network." June 2008.

[3] IEEE Std 242-2001 Buff Book – Protection and Coordination of Industrial and Commercial Power Systems.

[4] Tang, G. and Iravani, R. "Application of a Fault Current Limiter to Minimize Distributed Generation Impact on Coordinated Relay Protection." Presented at the International Conference on Power Systems Transients, 2005

[5] Prince Winston. D, Saravanan. M, "Review of Energy Saving Techniques for Three Phase Squirrel Cage Induction Motor Drive," Journal of Electrical Engineering, Pp 1-9

[6] S. Chekroun Et Al., "Development Of A Speed Sensorless Induction Motor Drives Using An Adaptive Neuro-Fuzzy Flux Observer," Journal of Electrical Engineering, pp 1-9.

[7] KLIMA, Jiri, "Analytical Investigation of an Induction Motor Drive Fed from VSI under Inverter Fault Conditions", International Conference on Electrical Engineering in 2008.

[8] M. S. Aspalli, Veerendra. D, P. V. Hunagund, A New generation VLSI approach for V/F control of Three-Phase Induction Motor. Proceedings of the International Conference on VLSI, Communication and Instrumentation, April7th -9th, 2011, Kottayam, India

[9] Alfredo, Thomas A. Lipo and Donald W. Novotny, "A New Induction Motor V/f Control Method Capable of High-Performance Regulation at Low Speeds" IEEE Trans. Industry Applications, Vol. 34, No. 4 July/ August 1998.