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Design of Single Edge Triggered Register Element Using Pseudo-NMOS Technique For Low Power Clocking Systems

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Abstract: Introduction: The flip-flops are considered as major contributors to the power dissipation of the clocking system, which is made up of the clock provision network and register elements (latches, flip-flops). **Methodology:** The power efficient Pseudo-NMOS based single edge triggered flip-flop is proposed by employing pseudo NMOS technique, split path and clock tree sharing methodologies for low power clocking systems. pseudo NMOS and split path techniques resolves floating node problem and short circuit power dissipation in latching part of the flip-flop respectively. For capturing the data D, clock tree sharing scheme allows the latching part of the flip-flop to share the clock provision network and reduces the number of transistors requirement to construct the clock provision network. Reduction of number of clocked loads is a methodology which minimizes the switching activity and reduces the dynamic power dissipation. This methodology is also employed in this proposed design to construct the latching part of the flip-flop. **Results:** The performance of flip-flop is analyzed by simulating the flip-flop circuit at 0.12μm CMOS process technology. The simulation comparison results that, the proposed design of register element achieves power saving from 8.06 to 42.83% , Improvement of power Delay Product from 66.86 to 81.26 % ,Energy Delay Product from 87.86 to 92.4% and Power Energy Product (PEP) from 66.22 to 91.22% Compared to the existing flip-flops (SPGFF,POWERPC,HLFF,XCFF,SDFF,CDMFF, DDFF and CTS-DETFF). **Conclusion:** Because of minimum power consumption, speed and reduced circuit complexity this proposed single edge triggering register element (flip flop) may preferable for low power and high speed clocking systems.

Key Words: Digital CMOS, single edge triggering, Register Element (flip-flop), Low power**.**

1. INTRODUCTION

Earlier, the primary concerns of the VLSI circuit design were area, performance and cost; the power consumption was considered as secondary concern. Now, this trend is changed and the power consumption is considered as one of the major concerns in VLSI circuit modeling [1]. One reason is that the enhancement of chip scale of integration and the steady improvement of the operating frequency has made power consumption as a major concern in VLSI circuit design. The excessive power dissipation in integrated circuits discourages their use in a portable device and also causes overheating which degrades the system performance and lifetime. Power dissipation has a direct impact on the packaging cost of the chip and coding cost of the system [2,3]. All of these factors drive the VLSI system designers to consider the power dissipation as a major issue and to reduce the circuit power dissipation.

The clocking system is one of the major power consuming components in VLSI system [4,5]. In the total power dissipation of the system, it accounts for 30% to 60% of power consumption [6], Power consumption of a particular clocking system can be represented as [7,8].

$$P_{clk-system} = P_{clk-tree} + P_{registerelements[ff]} \quad (1)$$

Where $P_{clk\text{-}tree}$ and $P_{register\ elements}$ represents power consumed by the clock allocation tree and register elements (flip-flops) respectively. The power consumed by the clock allocation tree can be expressed as:

$$P_{clk-tree} = \{(C_{line} + C_{clk-tsr}) V^2_{clk-swing}\} * f_{clk} \quad (2)$$

Where C_{line} is the interconnect line capacitance, $C_{clk\text{-}tsr}$ is the capacitance of clocked transistors of the register elements, $V^2_{clk\text{-}swing}$ is the clock swing voltage and f_{clk} is the clock frequency.

The power consumed by the register elements can be expressed as:

$$P_{registerelement[ff]} = \{(\alpha_i c_i \beta + \alpha_0 c_0 \beta_0 + C_{clk-Buf}) * V^2_{dd}\} * f_{clk} \quad (3)$$

Where α_i is the switching activity ratio of internal node, α_o is the switching activity ratio of output node, c_i is the internal node capacitance of the register element, c_o is the output capacitance of the register element, $C_{clk\text{-}Buf}$ is the capacitance of the clock buffers inside the register elements, f_{clk} is the clock frequency β is the trigger factor. β is 1 for single-edge triggering flip-flops and β is 2 for double-edge triggering flip-flops. Thus it is important to reduce the power consumption in both the clock allocation tree and register elements (flip-flops). As a result reduction of the power consumed by the flip-flops will have deep impact on the total power consumption of the clocking system [6].

In many existing microprocessors and digital applications master-slave and pulse-triggered flip-flops are selectively used. Conventional master-slave flip-flop is designed by the pair of latch, where one is transparent high and the other is transparent low [9,10]. It may be single edge triggered or double edge triggered. They are characterized by hard edge properties such as positive setup time causes large D to Q delay. Another edge triggered flip-flop is the sense amplifier based flip-flop SAFF [11,12]. Pulse triggered flip-flops reduce the two stages into one stage and characterized by soft edge property that is; negative setup time causes small D to Q delay. They could be classified into two types. The implicit pulse-triggered flip-flops [13] and the explicit pulse- triggered flip-flops [14]. There are three sources of power dissipation in a digital CMOS circuit. Static, dynamic and short circuit power dissipation. Total power dissipation of clocking system can be expressed as [4].

$$P_{total} = P_{static} + P_{dynamic} + P_{shortcircuit} \quad (4)$$

P_{static} is the static power dissipation which is caused due to leakage current or other current drawn continuously from the power supply. $P_{dynamic}$ is the dynamic power dissipation which is caused switching transient current and charging and discharging of load capacitance. $P_{shortcircuit}$ is the short circuit power dissipation due to short circuit currents that flow directly from supply to ground when n-sub network and the p-sub network of a CMOS gate both conduct simultaneously.

Power consumption of the clocking system is determined by the golden equation with the factors of switching activity (α), capacitance (c), supply voltage (v), frequency (f).

$$P_{dynamic} = \alpha C V^2 f \quad (5)$$

Based on these factors, there are various methodologies to reduce the power consumption shown as follows:

- Reducing capacity of clocked load
- Low Swing Clocking,
- Reducing the Transient Activity
- Reducing Short Current Power
- Reducing Leakage and Static Current
- Reducing the Capacitance
- Split path technique.

Power consumption of the flip-flop can be reduced by employing these methodologies. The existing flip-flops such as Symmetric Pulse Generator Flip Flop (SPGFF) [15], Power PC[9], Hybrid Latch Flip Flop (HLFF) [13], Cross Charge Control Flip Flop (XCFF) [16], Semi Dynamic Flip Flop (SDFF)[17], Conditional

Data Mapping Flip Flop (CDMFF) [18], Clock Tree Shared Double-Edge Triggered Flip-Flop (CTS-DETFF)[19] and Dual Dynamic node Flip Flop (DDFF) [20] are referred with its total number of transistors and clocked loads.

2. Pseudo-NMOS LOGIC

Principally NMOS logic family uses only n-type Field Effect Transistors (nFET) for circuit design. In the past, NMOS preceded CMOS technology is dominant one, but now it is obsolete. Pseudo - NMOS logic is a CMOS technique in which the circuits are similar to the older nFET-only NMOS logic family networks [21]. Basic NMOS inverter is shown in Figure 2.1. This uses a single NMOS transistor as a driver device that controls the inverter circuit. The load resistor R_L acts as pull-up device and is connected to the power supply V_{DD}. It always pulls-up the output voltage up to a value of V_{DD}. In Pseudo-NMOS logic, the load transistor R_L is replaced by always biased-ON PMOS transistor as demonstrated in Figure 2.2 and 2.3. Logic formation is achieved using only by the NMOS logic array and it pulls down the circuit to ground V_{SS}. this logic has no PMOS transistors in the logic array, leads to simplified interconnect wiring. This is the primary advantage of this logic.

The main advantage of this logic is it utilizes only N+1 numbers of transistors versus 2N numbers of transistors for static CMOS logic [22]. This logic efficiently avoids the floating node problem in the intermediate node between input and output node of the logic circuit. In this logic for all gates, high output voltage is equal to V_{DD} and low output voltage is not equal to 0 volts. This results in decreased noise margin.

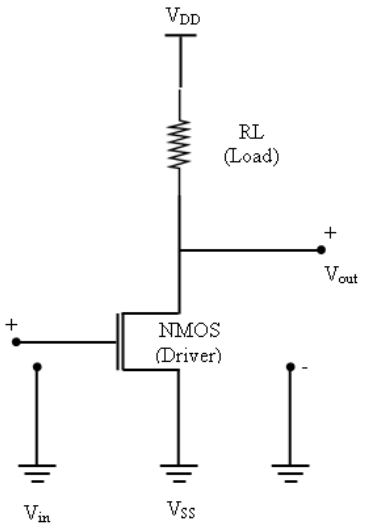

Figure 2.1 Basis NMOS inverter

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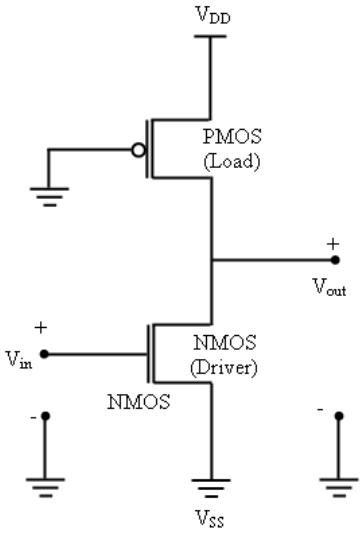

Figure 2.2 Inverter with pseudo-NMOS logic

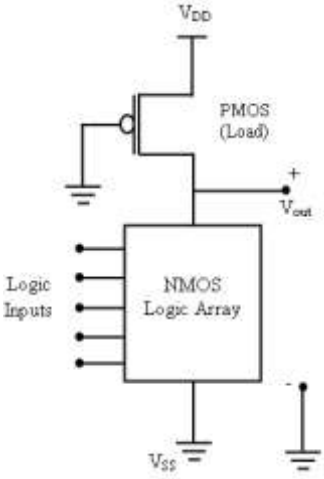

Figure 2.3 NMOS logic array with pseudo-NMOS logic

The main problem in this logic is the static power dissipation that occurs whenever the pull-down NMOS logic network turned ON. due to always ON PMOS transistor, while NMOS pull-down network is ON, there exists a direct current flow between V_{DD} and V_{SS} ground. In order to minimize the low output voltage as small as possible and to reduce the static power consumption, the ratioed transistors to be used for circuit design. For this logic the transistors should be properly sized to ensure the correct noise margin [23].

3. PROPOSED PN-SETFF REGISTER ELEMENT.

The Pseudo NMOS based Single Edge Triggered Flip-Flop (PN-SETFF) is proposed in this section. It captures the input data only at positive edge of the clock signal (CLK=1). It is constructed by two sections, latching and clock allocation section and required totally 12 numbers of transistors. This flip-flop uses 4 numbers of clocked transistors among total 12 transistors and it is illustrated in Figure 3.1. The numbers of clocked load is reduced in proposed flip-flop. Reducing the numbers of clocked loads reduces the switching

activity in this design. Because the switching activity of clocked transistor is very high compare to unclocked transistors [2, 3].

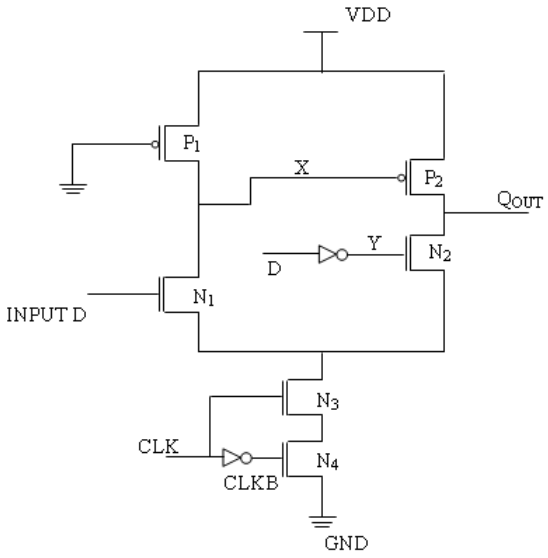

Figure 3.1 Pseudo NMOS based Single Edge Triggered Flip-Flop (PN-SETFF)

The latching section is made up of two stages. First stage is constructed by the transistors P1&N1, Second stage by P2&N2. The Pseudo NMOS technique is employed in this design at first stage of latching section. P1 transistor in the first stage is always ON transistor due to its permanent grounded gate [20]

The internal node X, which is present between first and second stage is charged to supply voltage V_{DD} through always ON Pseudo NMOS transistor P1. Hence node X always stays connected between the latching stages and will not be a floating node. The floating node problem is avoided in this PN-SETFF design.

The split path approach is another power reduction technique and employed in this flip-flop design. The NMOS transistor N2 is present in the outer discharge path of second latching stage. An intermediate node X only drives the PMOS transistor P2 and does not drives N2 discharging transistor. An inverter I1 is asserted by the input data D and provides the signal to the node Y. The node Y drives only the discharge NMOS transistor N2. Hence the transistors P2 and N2 in the second latching stage are driven by two separate signals from node X and Y respectively. This avoids the possibility of shorting the transistors P2 & N2, reduces the short circuit power dissipation.

In this design the clock allocation network is constructed by the pair of NMOS transistors N3 & N4. Clock allocation network sharing scheme is also used in this design. Two latching stages P1, N1 & P2, N2 share the clock allocation network for sampling the input data D. This sharing scheme reduces the number of transistors requirement for clock allocation network construction and reduces power consumption of clock allocation network.

The operation of this proposed element is as follows, when D=HIGH(1) ,CLK rises then CLKB will stay high for a short interval time which is equal to one inverter delay. During this period the clocked branch NMOS transistors (N3 & N4) turns ON and the flip flop will be in the period of evaluation. Among the

two stages in the latching part, first stage is responsible for loading 0 to 1 data input transition. The internal node X will discharge and causes the output Q=1. When CLK falls, CLKB will rise then D input stays HIGH (1). In this condition the first stage is disconnected from the ground then prevents the node X from redundant switching activity. The second stage is responsible for capturing the data transitions of 1 to 0. In this transition the pull down network of second stage to be ON, then it causes output Q=0.

The Pseudo NMOS technique, clock sharing and split path schemes reduces the overall power consumption of PN-SETFF.

4. RESULTS AND DISCUSSION

The simulation results are obtained from DSCH & MICROWIND simulations in 0.12 μm CMOS process technology at room temperature. Each circuit design is simulated at the layout level. In modern digital CMOS logic design, when the clock have an activity factor of about 1 then, it has a typical activity factor of about 0.1. In this design those transistors, in the clock pulse generator and also within the logic branch that are directly driven by the clock considered as 100% switching activity transistors.

The clock frequency is maintained as 125 MHz. The input data D (0, 1) is supplied alternatively to the circuit and verified its functionalities. The power consumption of the circuits is measured. Delay is measured from data to output (D to Q delay).

The conventional design optimization metrics to minimize the both power and delay of the electronic designs is power delay product PDP. It is referred as energy metric. If D represents delay and P represents power consumption of the circuit then the metric can be expressed as PDP(energy) = Power (P) × Delay (D) It gives balanced geometric weights to power and delay. PDP optimizes both power and delay equally.

EDP is a useful metric for evaluating the quality of the design [24]. It is expressed as EDP= Energy × Delay; EDP=P×D×D, But it may not be appropriate when the low power dissipation is priority. Because EDP gives a higher geometric weighting to delay than power. This metric is more suitable when the performance is the main concern.

PDP gives equal priority to both power and delay. EDP gives more priority to delay than power. If power is the higher priority then, both EDP and PDP matrices may not provide better solutions. For that the new metric power energy product PEP is considered [25]. It gives higher geometric weight to power than delay and produces lower power solution than the other two matrices. It is expressed as PEP = Power × Energy; PEP = P×P×D.

In SETFF the data is sampled at either positive or negative edges of the clock arrivals. The proposed PN-SETFF samples the input data D at positive edge of the clock signal and the functionality of the proposed circuits is checked for four cases.

Operation (1):

Input data D=1, CLK=1, CLKB=0; output Q=1 & Qb= 0

Operation (2):

Input data D=1, CLK=0, CLKB=1; output Q=0 & Qb= 1

Operation (3):

Input data D=0, CLK=1, CLKB=0; output Q=0 & Qb= 1

Operation (4):

Input data D=0, CLK=0, CLKB=1; output Q=0 & Qb= 1

The schematic diagram for proposed PN-SETFF design in DSCH tool is shown in Figure 4.1. The above mentioned functionality of proposed register element is checked under different set of input D and CLK signals and shown in Figure 4.2, 4.3, 4.4, and 4.5 respectively. Output waveform of proposed PN-SETFF with Power consumption is shown in Figure 4.6 and its physical layout is shown in Figure 4.7.

The performance parameters such as total number of transistors, number of clocked transistors, Layout area (A), power consumption (P), Delay (D-Q), and optimization metrices such as Power Delay Product (PDP), Energy delay product (EDP), Power energy product (PEP) are taken to evaluate the significance and potential of the proposed flip flop design with the existing designs.

Table 4.1 & 4.2, 4.3 & 4.4 demonstrates the results of existing register elements and proposed PN-SETFF design in terms the performance parameters, optimization metrices respectively. For a clear comparison the Bar charts are given for the performance parameters such as, Number of transistors and Number of clocked loads Figure 4.8, Layout area Figure 4.9, Power consumption Figure 4.10, Delay Figure 4.11, and also given for optimization metrices such as PDP, EDP and PEP Figure 4.12.

Table 4.1 Performance Parameters Comparison of Existing Register Elements

Register Elements	**Performance parameters**					
	Total No. of Transistors	**No. of clocked transistors**	**Triggering mode**	**Area (μm^2)**	**D -Q Delay (ps)**	**Total Power (μw)**
SPGFF	30	16	Double	546	162	16.4
POWER PC	22	8	Single	429	176	13.424
HLFF	20	10	Single	312	158	12.276
XCFF	21	4	Single	338	163	11.123
SDFF	23	7	Single	264	156	11.028
CDMFF	22	7	Single	429	178	10.277
DDFF	18	6	Single	299	166	9.725
CTS-DETFF	23	8	Double	424	179	8.347

Table 4.2 Optimization Metrices Comparison of Existing Register Elements

Register Elements	**Optimization metricies**		
	PDP (fj)	**EDP ($\times 10^{-24}$)**	**PEP ($\times 10^{-20}$)**
SPGFF	2.656	0.430	4.355

POWER PC	2.362	0.415	3.170
HLFF	1.939	0.306	2.380
XCFF	1.813	0.295	1.135
SDFF	1.720	0.268	1.896
CDMFF	1.829	0.325	1.879
DDFF	1.614	0.267	1.131
CTS-DETFF	1.503	0.2690	1.263

Table 4.3 Performance parameters of proposed register element PN-SETFF

Performance parameters	**Proposed Register Element PN - SETFF**
Total No. of Transistors	12
No. of clocked transistors	4
Triggering mode	Single
Area(μm^2)	182
D –Q Delay (ps)	65
Total Power (μw)	7.647

Table 4.4 Optimization metrices of proposed register element PN-SETFF

Optimization Metrics	**Proposed Register Element PN - SETFF**
PDP (fj)	0.498
EDP ($\times 10^{-24}$)	0.0324
PEP ($\times 10^{-20}$)	0.382

By comparing the Table 4.1 and 4.3, In view of total number of transistors, the proposed PN-SETFF uses 4 clocked loads among totally 12 numbers of transistors. This is minimum number of transistors count compare with existing register elements in Table 4.1. PN-SETFF achieves 33.33% to 60% of total

number of transistors reduction compare with existing and CTS-DETFF register elements and achieves 33.33% to 75% of clocked transistors reduction compared to CTS-DETFF and existing register elements in Table 4.1 except XCFF. The register element XCFF consists of 4 numbers of clocked loads which is equal to clocked load counts of proposed PN-SETFF.

The proposed PN-SETFF design resolves the floating node problem effectively by following Pseudo NMOS technique. The internal node X, which is present between first and second stage is charged to supply voltage V_{DD} through always ON Pseudo NMOS transistor P1. Hence node X always stays connected between the latching stages and will not be a floating node. The Pseudo NMOS technique efficiently avoids the floating node problem in proposed PN-SETFF design.

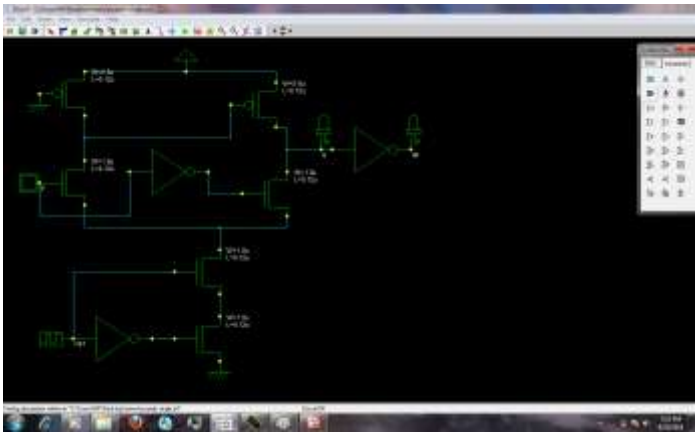

Figure 4.1 Schematic diagram of proposed PN-SETFF

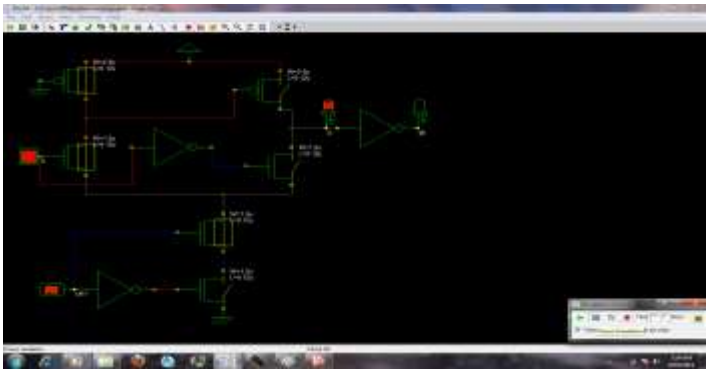

Figure 4.2 Operation (1): (input data D=1, CLK=1, CLKB=0; output Q=1 & Qb= 0)

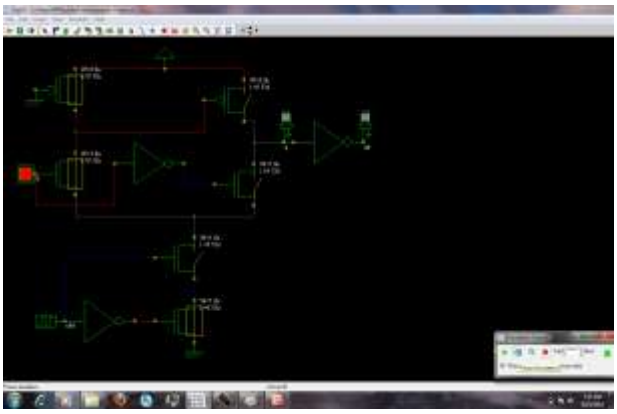

Figure 4.3 Operation (2): (input data D=1, CLK=0, CLKB=1; output Q=0 & Qb= 1)

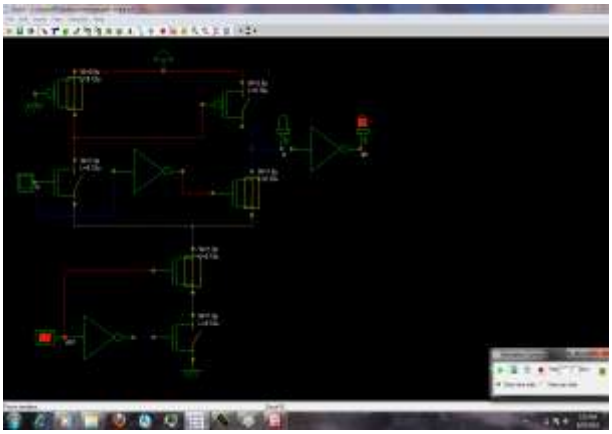

Figure 4.4 Operation (3): (input data D=0, CLK=1, CLKB=0; output Q=0 & Qb=1)

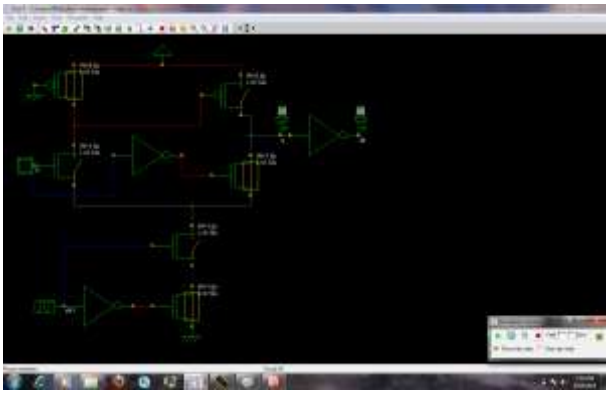

Figure 4.5 Operation (4): (input data D=0, CLK=0, CLKB=1; output Q=0 & Qb= 1)

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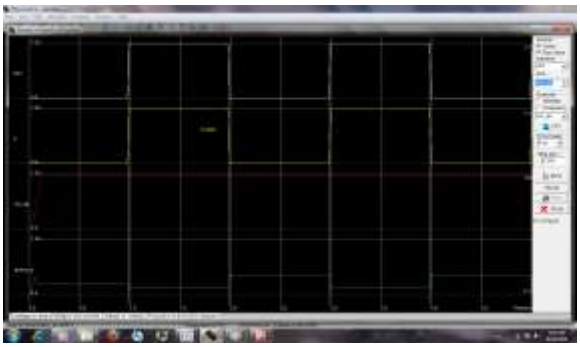

Figure 4.6 Output waveform of proposed PN-SETFF (Power consumption = 7.674µw)

The proposed PN-SETFF has the area of 182µm^2. This proposed design occupies minimum area and achieves 31.06% to 66.66% of less area, Compare to existing register elements and CTS-DETFF. In view of D-Q delay, the proposed PN-SETFF has the delay of 65ps. This delay value is very less compare to existing register elements and CTS-DETFF.

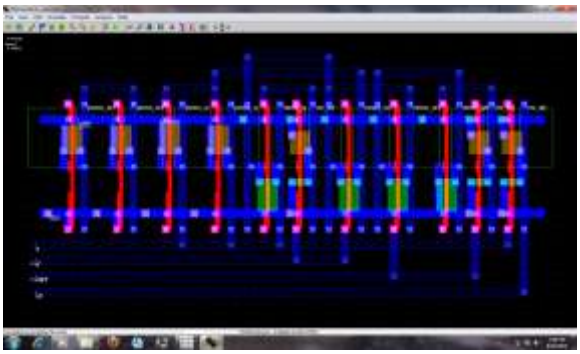

Figure 4.7 Physical Layout of proposed PN-SETFF (area= 182µm^2)

In terms of total power consumption, the proposed PN-SETFF consumes the total power of 7.674µw. Compare to all existing register elements in Table 4.1.This proposed design achieves 8.06% to 42.83% of power reduction.

By comparing the Table 4.2 and 4.4, In point of PDP, the proposed PN-SETFF has the PDP value of 0.498 fj. It is improved 66.86% to 81.25%, compare to all existing flip-flops in Table 4.2. In view of EDP, the proposed PN-SETFF has the value of 0.0324×10^{-24}. Compare to all existing flip-flops and CTS-DETFF the EDP value for this proposed PN-SETFF is improved from 87.86% to 92.46%. In point of PEP, the proposed PN-SETFF has the value of 0.382×10^{-20} and improved 66.22% to 91.22% compare to existing flip-flops and CTS-DETFF register element.

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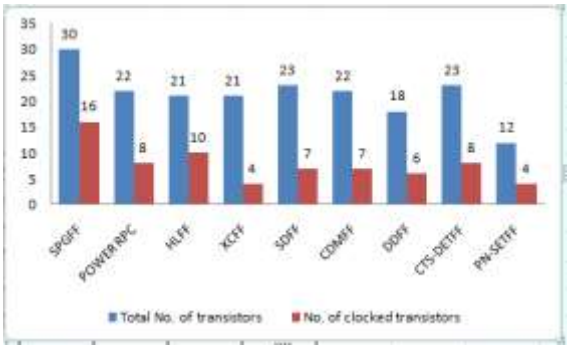

Figure 4.8 Comparison of total number of transistors and number of clocked transistors

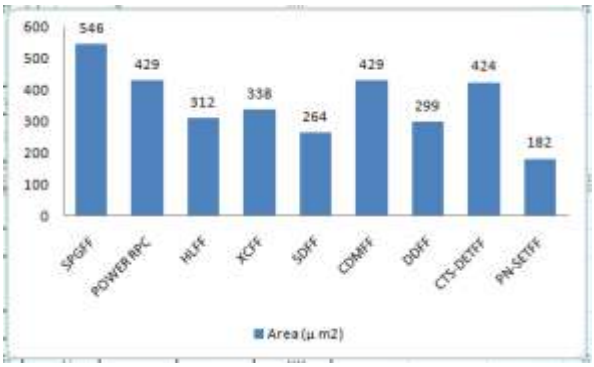

Figure 4.9 Comparison of layout area occupation

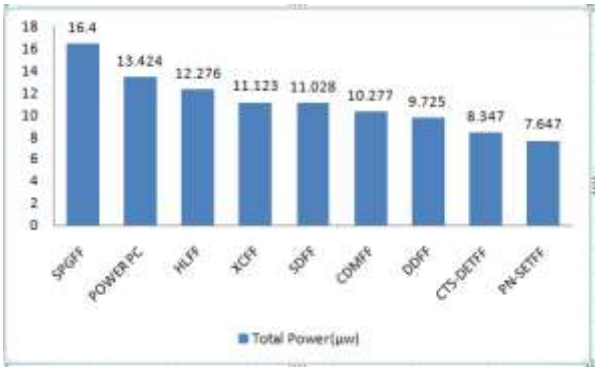

Figure 4.10 Comparison of total power consumption

Figure 4.11 Comparison of D-Q delay

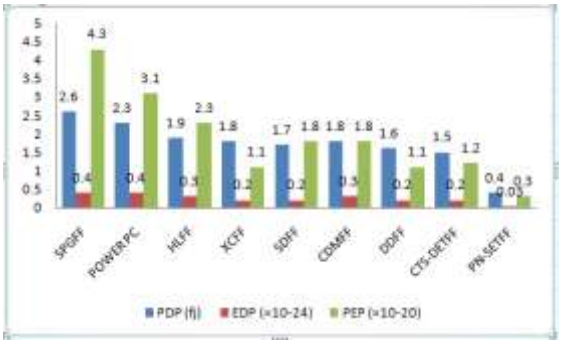

Figure 4.12 Comparisons of Power Delay Product (PDP), Energy Delay Product (EDP) and Power Energy Product (PEP)

4.4 CONCLUSION

In this article, Pseudo NMOS based Single Edge Triggered Flip-Flop (PN-SETFF) is described for low power clocking system. This register element is designed by following Pseudo NMOS technique and resolves the floating node problem effectively. It employs split path technique, reduces the short circuit power dissipation. In this design the number of clocked transistors is reduced as 4 transistors by following the method of reducing the numbers of clocked loads. The switching activity of clocked transistor is very high compare to unclocked transistors. Reducing the numbers of clocked loads minimizes the switching activity in this design that reduces dynamic power dissipation. Clock provision network sharing scheme is also used in this design .Both first and second latching stages in this flip-flop design shares the clock allocation network to capture the input data D. This sharing scheme reduces the number of transistors requirement to construct the clock allocation network and reduces the power consumption of clock allocation network.

It reduces the total power consumption of proposed PN-SETFF as 7.674μw and delay value as 65 ps. The optimization metrices of proposed PN-SETFF are improved as PDP = 0.498 fj, EDP = 0.0324×10^{-24} and PEP = 0.382×10^{-20}. Due to minimum power consumption and less delay compared with existing flip-flops and CTS-DETFF register element design, this proposed register element well appropriate for high speed and low power clocking systems design.

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