

Implementation of Ternary Logic in QCA using SPICE Macro-Modeling

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Abstract. In this paper, we introduce a new trend in Quantum dot Cellular Automata – Ternary QCA (tQCA) and have justified its presence using SPICE (Simulation Program with Integrated Circuit Emphasis). The macro-modeling which we have shown is concise and compact. Our proposed model for metal-island tQCA has helped to estimate its logic performance. This work sets a mark-up in the domain of cellular automata and it has shown that it can operate in the milli-volt (~60mV) regime.

Keywords: tQCA, SPICE macro-model of tQCA, tunnel junction, ternary logic.

1 Introduction

In engineering industry as well in the research field, the traditional integrated circuit (IC) technology is facing severe limitations to move further in advancement. Technologists have been searching for alternative and the things which came up in this process, were quite interesting. The reasons behind this fall down of traditional IC technology – CMOS, has been quite well explained in [1, 14] and there it has been stated that there are quite a good upcoming potential devices beyond CMOS [1].

But how to decide which one is the almost best amongst them. Even though, this finding is hard to make, various literatures [11, 12] suggest for Quantum dot Cellular Automata (QCA). Very smooth research works have been carrying on QCA, and excellent explorations have been done with

binary QCA (bQCA). Here, two polarized state has been observed viz. “+1.00” and “-1.00”, stating logic “1” and logic “0” respectively.

We think of multi-valued logic, especially ternary logic which can have potential advantages such as greater data storage capability, faster arithmetic operations, better support for numerical analysis, non-deterministic and heuristic procedures, communication protocol and an effective solution for non-binary problems [2-7]. Multi-valued logic, in form of ternary logic has been already implemented successfully on VLSI circuits [8].

Multi-valued logic (MVL) is growing in an extensive level in digital electronics. In accordance to conventional binary logic, multi-valued logic has higher information density. MVL has the ability to reduce the number of operations that is required to implement a particular mathematical function; thus it has an advantage in terms of reduced area, which in turn reduces the propagation delay and provides a higher speed of operation [19]. More importantly, an ‘e’ level system has low engineering costs as explained in [9]. Since the value of ‘e’ is 2.71828, nearest to 3, therefore, three level logic i.e., ternary logic has become quite popular. Nowadays, the QCA platform is being utilized to implement ternary logic. LebarBajec et al. [2], the pioneer of ternary QCA (tQCA), reported in 2006. In the Letter [10], one of us had proposed a quantum mechanical approach to calculate the physical properties of the ternary QCA (tQCA) cell, such as its material choice at room temperature, quantum dot dimension, cell size and its limitation to fabrication. Our work, focused on developing an electrical model of tQCA cell which will be competent to estimate the cell performance. In regard to this, we tried a physical analysis of the model, and extracted the tunneling resistance and capacitance. We used the SPICE to measure the behavior and a detailed analysis has been put on. In Section 1.1, we discuss on the bQCA and in section 1.2 we state the tQCA designed structures. The physical analysis of tQCA has been explored in Section 2 and its sub sections 2.1, 2.2 and 2.3. Rest of the paper, we highlight the simulation results supporting our observations in Section 3, and in Section 4, we give the conclusion of our work.

1.1 Binary QCA (bQCA)

The advent of QCA in 2005 was designated in the form of bQCA as two level logic got represented in it. Basically, bQCA has a structure with four quantum dots (QD) made with semiconductor or Metal Island or molecular redox. The four dots are positioned at the corner of a squared – shaped cell [10]. Each dot is separated from the other by tunnel junction. In IC technology when devices shrink in size, electron tunneling happens. This

tunneling junction controls the tunneling of electron from one dot to another dot. There is the influence of clock on the QDs. This clock is nothing but the tool to either lower down or higher up the potential barrier between the QDs. Actually, it help in determining the polarization of the cell and thereby the logic level. The free electron within the cell settles diagonally due to coulombic interaction. The left diagonal alignment of electron in bQCA cell is logic “0” and the right diagonal alignment is logic “1” as shown in figure 1(a). The bQCA in general has two types of cell alignment viz. 90-degree and 45-degree as shown in figure 1(b) [15].

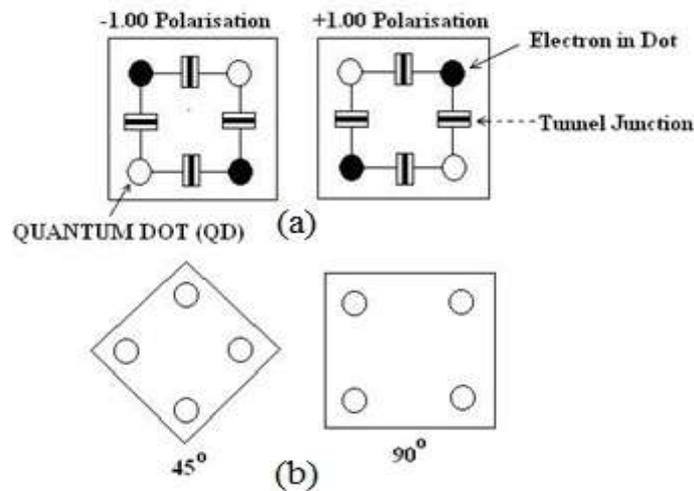


Figure. 1. (a) Basic bQCA cell with four QDs stating the polarizations: “-1.00” ~ logic ‘0’ and “+1.00” ~ logic ‘1’ (b) 45-degree & 90-degree alignment of bQCA cell.

1.2 Ternary QCA (tQCA)

The tQCA can be thought of as the merging of two bQCA alignments: 45-degree and 90-degree. The major difference between the tQCA cell and bQCA cell lies in the number of quantum dots and its polarization states. The classification of tQCA is same as bQCA viz. semiconductor-based tQCA, metal-island tQCA. The tQCA is realized by means of eight QDs within a square-shaped cell and two free electrons confined within the cell. Eight dots are arranged in ring shape within the square cell as shown in figure 2. The four polarized states of tQCA are “-1.00”, “+1.00”, “0.00” and “no polarization or neutral” represented by ‘A’, ‘B’, ‘C’ or ‘D’ and ‘N’ respectively. We have no electrons in the state “N” due to the absence of polarization. The device design of tQCA has many constraints such as temperature, size of cell, QD size etc., and these aspects are quite challenging to solve. To have a good logic paradigm for tQCA, these things are to be considered. The diameter of the ring must be equal to the length of

the squared cell. As a result, $R = L/2$, if 'R' be the radius of the ring and 'L' be the length of the squared cell. Therefore, the maximum distance of separation between two QDs is L. Advance lithography process like High-resolution electron beam lithography will be able to fabricate such a structure [20].

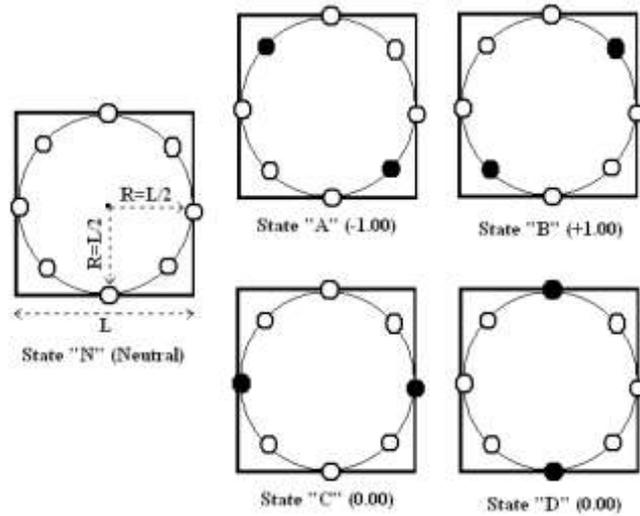


Figure. 2. Eight dot tQCA cell along with corresponding polarised and non-polarised states.

2 Physical Analysis of tQCA

As stated in [13], a quantum dot can be thought of as a site connected to drain and source via tunnel junction, as shown in fig. 3. The dot is actually a conductive island sandwiched between two tunnel junctions, which is kind of the implication of having potential barrier around the dot site.

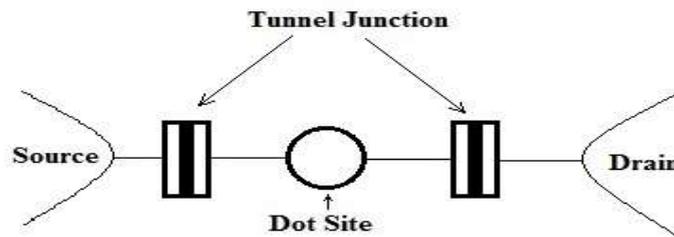


Figure. 3. Physical structure of a quantum dot.

The amount of energy (ΔE) needed for the movement of an electron from one dot site to another is designated as $\Delta E = \frac{e^2}{C_j}$, here e is the electronic charge equals to $1.60217657 \times 10^{-19}$ joules and C_j is the junction capacitance between two dots. The thing that happens is like pushing the free electron

within the cell, traversing from one dot site to the other. Tunnel junction is kind of the gateway regulating the flow of electron. In tQCA, the possible combination, we have worked on, depicts few projections in regard to determine the logic values. When the input to a clock is ‘F’, it indicates the tunnel junction corresponding to that clock is inactive as seen in fig. 5, meaning it does not allow any electron to pass through it [16]. For instance, see table 1, for the logic state ‘A’, there the inputs to clock-1, clock-2 and clock-4 are ‘F’ allowing only the tunnel junction T_{57} remain active. So, the free electron has the scope to move within the dot sites D-1, D-5, D-7 and D-8 as the other dot-sites are blocked. But the free electron will finally settle down at dot site D-5, so as to attain the maximum distance within two dot site because of coulombic interaction. Likewise, if we see for the logic state ‘B’, there the inputs to clock-1, clock-2 and clock-3 is ‘F’ allowing only the tunnel junction T_{68} remain active. Thereby, the electron can circulate within the dot sites D-2, D-6, D-8 and D-4 and will finally settle down at dot site D-6. In case of logic state “C or D”, the inputs to clock-2, clock-3 and clock-4 are ‘F’ letting only the tunnel junction T_{12} remain active. So, the free electron can live within D-5, D-1, D-2 and D-6 and the possibility being that the electron will settle at D-1 or D-2 as reported in [16].

Table 1. Logic Configuration of tQCA

S.No.	Clock-1	Clock-2	Clock-3	Clock-4	Logic State
1.	(F)	(F)	(R)	(F)	“A”
2.	(F)	(F)	(F)	(F)	“Neutral”
3.	(F)	(F)	(F)	(R)	“B”
4.	(F)	(F)	(R)	(R)	“Neutral”
5.	(R)	(F)	(F)	(F)	“C or D”
6.	(R)	(R)	(F)	(F)	“Neutral”
7.	(F)	(R)	(F)	(F)	“D or C”

For logic state “D or C”, inputs to clock-1, clock-3 and clock-4 are ‘F’ and so the tunnel junction T_{43} remains active. Therefore, the free electron can move within the dot sites D-7, D-3, D-4 and D-8 and the free electron can settle at the space of dot site D-3 or D-4.

2.1 SPICE analysis of tQCA

After speculating the behavior of QCA cells, it was reported in [18], that the cell is nothing but two series-connected metal dots separated by tunnel junction and capacitive coupled to the second pair of identical structure. Based on this notion, we have built the tQCA model. Taking the exhaustive results of the experiments carried out in [17], we have implemented them in our model. We have known from the previous section that the clock is the

instrument to control the flow of electrons and triggers the change in logic states. The clock has been appointed to regulate the work ability of tunnel junction (see figure 5). In literature survey, it was not clear as to how implement the tunnel junction in the form of active component as it plays a major role in determining the functionality of the cell. From [17], it was quite clear that the tunnel junction is $R_T \cdot C$ coupling, where R_T is the tunneling resistance and C is the tunneling capacitance. We have implemented R_T and C in parallel coupling for the tunnel junction in tQCA cell and observed satisfactory result in SPICE described in section 3.

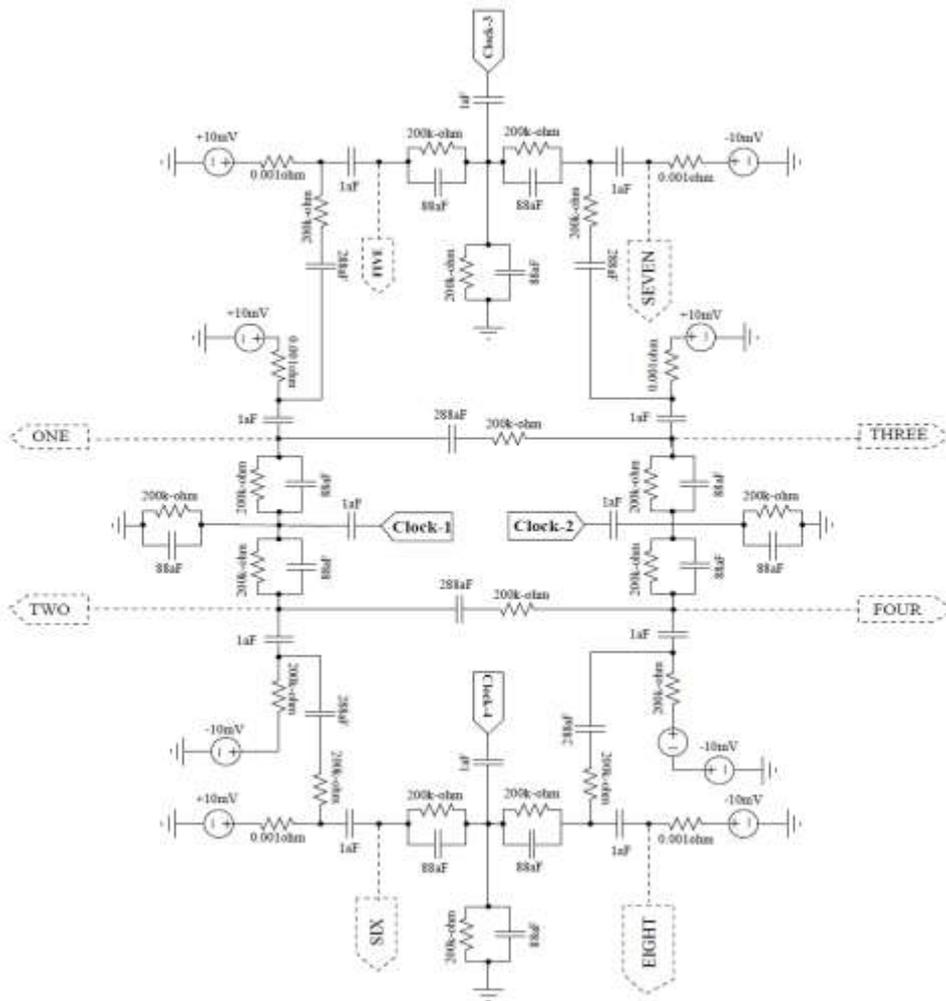


Figure 4. Schematic of tQCA using half cell

In SPICE, we have used the $R_T = 200k\Omega$ and $C = 88aF$ which is visible in figure 4, as these were the satisfactory values obtained from the experiment performed in [17]. Moreover, R_T is always tried to be kept way greater than

the quantum-hall resistance ($\sim 25.813\text{k}\Omega$) in order to make the cell work in room temperature. We have used the concept of half QCA cell as shown in [18] to build the eight dot tQCA cell as shown in figure 4.

2.2 Realization of tQCA

The formation of tQCA is done using Metal Island and small capacitance [16]. Through the tunnel junction as mentioned earlier only few electrons get to tunnel in and out from the metal-island QD at an instantaneous time. The charge configuration of system is composed of control electrode or clock and the QD, coupled by tunnel junctions and capacitance as shown in figure 5. The capacitances in figure 5 are the passive connectors between the dot sites whereas the tunnel junctions are their corresponding gateways. The electrostatic energy (E) of charge configuration system can be expressed in terms of voltage and charge as shown equation 1:

$$E = \frac{1}{2} \begin{bmatrix} q \\ q' \end{bmatrix}^T C^{-1} \begin{bmatrix} q \\ q' \end{bmatrix} - v^T q' \quad (1)$$

where, C is capacitance matrix, v is column vector of voltage source; q, q' are column vector of island charge and lead charge.

2.3 Model for logic value configuration of tQCA

Basically, the model we present here is a model for the metal-island tQCA. We tried to frame the eight dot structure of tQCA on SPICE platform. The tQCA cell has four control knobs or clocks to operate its polarization while interacting with its neighbor cell. The model has eight quantum dot sites (i.e., D-1, D-2, D-3, D-4, D-5, D-6, D-7, and D-8) where the free electrons can live depending on the input voltage on the clock. C_j is the junction capacitance between the dots. The tunnel junction provides the potential barrier to the electron transport and is an important criterion in tQCA. The positional instances of the electrons on the dots determine the logic state of the cell. The clock inputs (clock-1, clock-2, clock-3, and clock-4) have been altered, issuing them with possible rising pulse (R) and falling pulse (F) combination and obtained the logic states as stated in Table 1. The implemented clock triggers at 5ns, and the electron gets trapped.

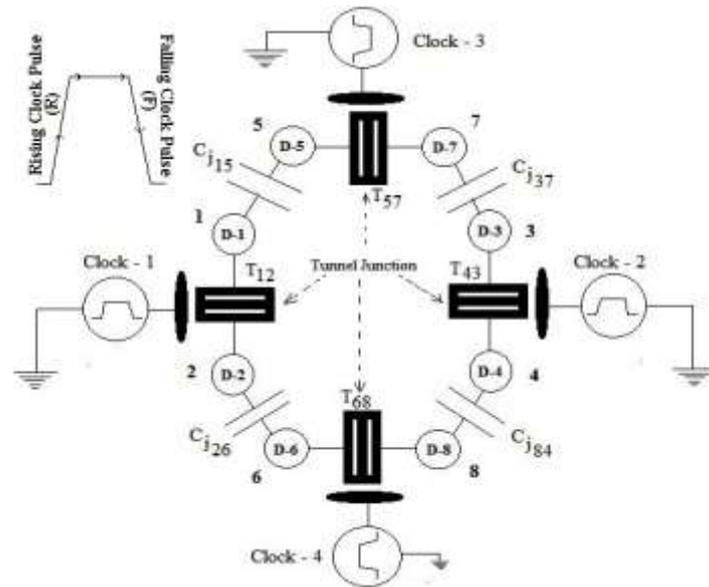


Figure 5. Modelling for metal-island tQCA

3 Results and Discussions

The things we have discussed in Section II were quite noteworthy for tQCA. To verify those observations, we tried some analysis on SPICE. We measured the potential differences at the dot site D-5, V(five) and the dot site D-8, V(eight), finding V(five) greater than V(eight) which directs to the fact that the presence of electron is at D-5. Though the magnitude of V(five) and V(eight) are same, the positive voltage of V(five) indicates the quicker settlement of electron at the dot-site D-5 compared to the electron possibly be settling at D-8 as shown in figure 6.

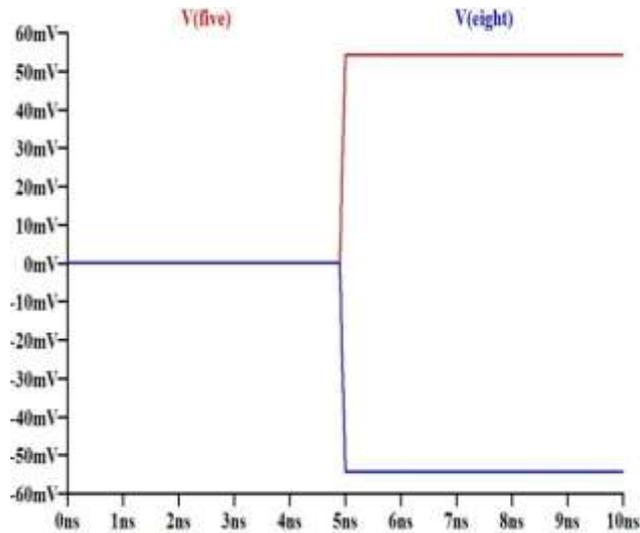


Figure. 6. SPICE simulation for logic state ‘A’

This conforms the logic state ‘A’ to polarization “-1.00”. In the same fashion, the potential difference at D-8 is greater than potential difference at D-5, when the clock inputs are altered in accordance to table 1. Thereby, it indicates the quicker settlement of electron at the dot-site D-8 compared to D-5, even though their voltage magnitudes are same as shown in figure 7.

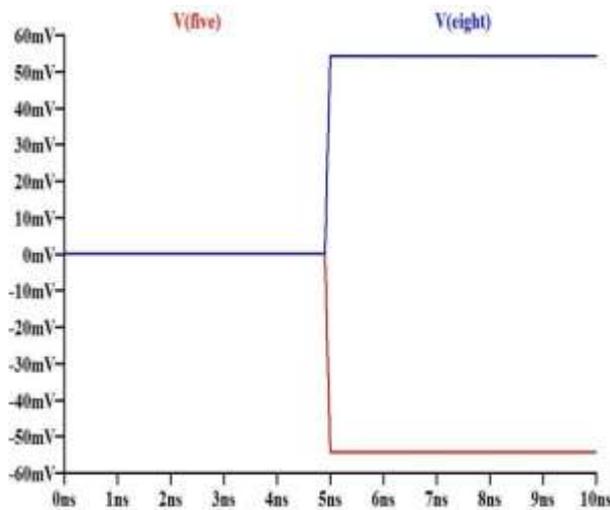


Figure. 7. SPICE simulation for logic state ‘B’

This declares the happening of logic state ‘B’ with polarization (+1.00). Till here, it was quite known due to the knowledge from the behavior of bQCA. The interesting part is now when we find two other logic states giving a good

justification to the name “tQCA”. We report of seeing two unknown logic states namely ‘C’ & ‘D’ by altering the clock inputs as directed in table 1 [16]. On seeing the simulation in fig. 8, it gets visible that the potential at D-1 and D-2 are positive, but is having different magnitudes.

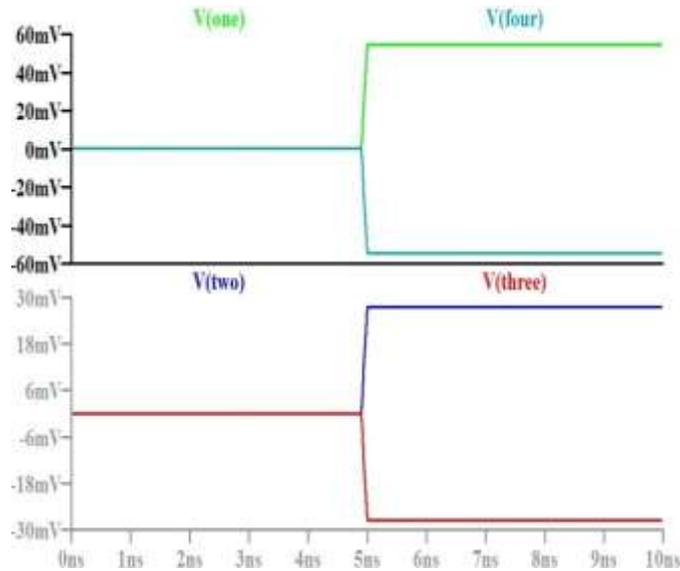


Figure. 8. SPICE simulation for logic state ‘C or D’

Now, this indicates the electron being settling quicker at either D-1 or D-2. So, the logic state is referred as “C or D” with polarization ‘0.00’. If the electron is at D-2, the locked electron will be at D-3 to have a best coulombic interaction and this can be also likely to be said as potential difference at D-3 is at approximately -30mV (same but negative voltage as D-2). Similarly, if the electron is at D-1, the other electron gets trapped at D-4 as seen in figure 8.

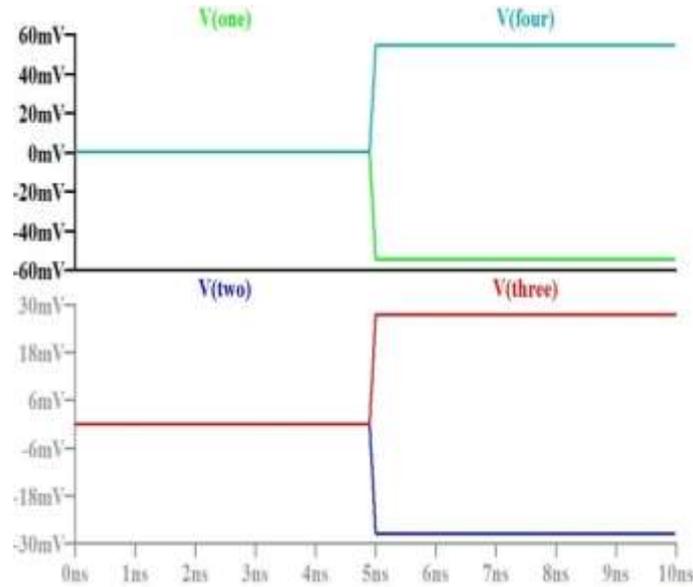


Figure. 9. SPICE simulation for logic state ‘D or C’

We obtain another indeterminate logic state with polarization “0.00” and reasoning of it is same as the previous one as seen in figure 9.

4 Conclusions

Though the traditional quantum dot cellular automata, bQCA is a very new technology, but it does not show feasibility in defining more than two logic levels. In this respect, tQCA has shown its compatibility through our work. We were able to focus on the performance estimation of tQCA using a very powerful tool SPICE. All the simulations were carried on LTspiceIV and the analysis have shown that tQCA operates in the milli-volts range ($\sim 0 - 60$ mV), proving its possibility to be used for low power applications in near future. Since QCA is a technology based on quantum confinement within a closed dimension [11], therefore there lies no question of power leakage, proving that it has minimum static power dissipation.

REFERENCES

- [1] Haron, N. Z., and S. Hamdioui. "Why is CMOS scaling coming to an END?." Design and Test Workshop, 2008. IDT 2008. 3rd International. IEEE, 2008.

- [2] LebarBajec I., Zimic N., Mraz M.: 'The ternary quantum-dot cell and ternary logic', *IOP Nanotechnol.*, 2006, 17, (8), pp. 1937–1942.
- [3] Pecar P., Mraz M., Zimic N., Janez M., Bajec I.L.: 'Solving the ternary QCA logic gate problem by means of adiabatic switching', *Jpn. J. Appl. Phys.*, 2008, 47, (6), pp. 5000–5006.
- [4] Pecar P., Ramsak A., Zimic N., Mraz M., LebarBajec I.: 'Adiabatic pipelining: a key to ternary computing with quantum dots', *IOP Nanotechnol.*, 2008, 19, (49), pp. 495401.
- [5] LebarBajec I., Pecar P.: 'Two-layer synchronized ternary quantumdot cellular automata wire crossings', *Nanoscale Res. Lett.*, 2012, 7, p. 221, doi:10.1186/1556-276X-7-221.
- [6] Pecar P., LebarBajec I.: 'The key elements of logic design in ternary quantum-dot cellular automata', *Unconventional computation, Lect. Notes Comput. Sci.*, 6714, 2011, pp. 177–188, doi:10.1007/978-3-642-21341-0_21.
- [7] Shi-Yan Y., Tai-Yi P., Lin-Rong X.: 'A simulation of basic logic circuit based on ternary quantum-dot cellular automata'. *IEEE Proc. 30th IEEE Chinese Conf. on Control Conference*, 2011, pp. 5324–5327.
- [8] Smith, Kenneth C. "The prospects for multivalued logic: A technology and applications view." *Computers, IEEE Transactions on* 100.9 (1981): 619-634.
- [9] Wu, X. W., and F. P. Prosser. "CMOS ternary logic circuits." *IEEE Proceedings G (Circuits, Devices and Systems)* 137.1 (1990): 21-27.
- [10] Das, Kunal, Debashis De, and Mallika De. "Realisation of semiconductor ternary quantum dot cellular automata." *Micro & Nano Letters, IET* 8.5 (2013).
- [11] Cole, T., and J. C. Lusth. "Quantum-dot cellular automata." *Progress in Quantum Electronics* 25.4 (2001): 165-189.
- [12] Navi, Keivan, et al. "A new quantum-dot cellular automata full-adder." *Microelectronics Journal* 41.12 (2010): 820-826.
- [13] Mahapatra, Santanu, et al. "Analytical modeling of single electron transistor for hybrid CMOS-SET analog IC design." *Electron Devices, IEEE Transactions on* 51.11 (2004): 1772-1782.
- [14] Bhattacharjee, Pritam, and Arindam Sadhu. "VLSI Transistor and Interconnect Scaling Overview." *Journal of Electronic Design Technology* 5.1 (2014): 1-15.
- [15] Antonelli, Dominic A., et al. "Quantum-dot cellular automata (QCA) circuit partitioning: problem modeling and solutions." *Proceedings of the 41st annual Design Automation Conference. ACM*, 2004.
- [16] Bhattacharjee, P., Das, K., De, M., & De, D. (2015). SPICE Modeling and Analysis for Metal Island Ternary QCA Logic Device. In

Information Systems Design and Intelligent Applications (pp. 33-41). Springer India.

- [17] Bonci, L., et al. "Simulation of time evolution of clocked and nonclocked quantum cellular automaton circuits." *Journal of applied physics* 92.6 (2002): 3169-3178.
- [18] Tang, Rui, Fengming Zhang, and Yong-Bin Kim. "Quantum-dot cellular automata SPICE macro model." *Proceedings of the 15th ACM Great Lakes symposium on VLSI*. ACM, 2005.
- [19] Gang, Wu, Cai Li, and Li Qin. "Ternary logic circuit design based on single electron transistors." *Journal of Semiconductors* 30.2 (2009): 025011.
- [20] Hu, Wenchuang, et al. "High-resolution electron beam lithography and DNA nano-patterning for molecular QCA." *Nanotechnology, IEEE Transactions on* 4.3 (2005): 312-316.